Fabrication and Characterization of GaP/Si Nanodiode Array Based on Nanowires Synthesized from GaP Epilayers Grown on Si Substrates

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Abstract

Since many decades, the hope towards achieving an integration of III−V semiconductor materials with silicon has seemed to be a reachable goal, despite the existence of many challenges, represented by generation of various crystalline defects. Although the lattice mismatch between GaP and Si is relatively small, the large difference between their thermal expansion coefficients is the most important reason for the formation of defects, such as dislocations.

In this work, epitaxial growth of GaP/Si heterostructures for the fabrication of low-noise GaP/Si nanodiode array based on nanowires, using the top-down etching technique, is reported. The grown films were characterized using X-ray diffraction (XRD), scanning-electron microscopy, atomic-force microscopy and electrical measurements, which include current-voltage and capacitance-voltage measurements. Besides that, the interface between the epilayer and the substrate was deeply studied using a low-frequency noise (LFN) spectroscopy.

The GaP layers were grown on p-type Si (100) substrates using a Riber-32P gas-source molecular-beam epitaxy system. The dependence of surface morphology and crystal quality on the growth conditions, such as growth temperature, was intensively investigated for minimizing the defects. Therefore, the heterostructure films were grown at substrate temperatures of 550, 400 and 250 °C with a nominal thickness of 500 nm. The optimal growth temperature was then found to be 400 °C. Nevertheless, very poor-quality films, with high-density dislocations were obtained. Accordingly, in order to improve the crystal quality, the system in situ was subjected to thermal annealing at a temperature of 500 °C for 10 min. Due to such annealing, the layer quality exhibited a very slight improvement. Hence, a new thermal annealing method was proposed, and intentionally referred to as step-graded annealing (SGA) in this thesis. In this method, the temperature was increased gradually from 400 to 480 °C for 90 min, while the film was monitored by reflection high-energy electron diffraction (RHEED) the entire annealing process. Surface reconstructions in situ during the annealing were monitored by RHEED, which indicated to a high improvement in the crystal quality. The lattice parameters of GaP were then measured by asymmetric

XRD, and found to be equal to the bulk GaP exactly. By applying this method, the epilayer was found to be n-type auto-doped, and exhibited diode rectification behaviour.

Interesting information about the trap levels generated in the heterostructure films was revealed via LFN measurements. For instance, in one of the unannealed samples, two trap levels in the band gap were determined. Thereby, with the help of the SGA method, free-trap system with low-level noise was obtained.

Thereafter, electron-beam lithography (EBL) was used for printing nanopatterns on the surfaces, as a step for the fabrication of GaP nanowires. Because the surface of GaP substrate is very smooth in comparison to the surface of epilayer, it was used for the optimization of the EBL process. Gold mesh with high density holes of diameters about 200 nm was fabricated on the GaP substrates, which was then successfully transferred to the GaP layers.

The so called metal-assisted chemical etching (MacEtch) technique has recently been proposed and becoming much preferable for the nanowires fabrication. But, this method is still very limited to III−V compounds. Therefore, fabrication of GaP nanowires by this technique was a large challenge. To avoid the effect of crystalline defects on the etching results, such as the roughness of the surface, the MacEtch process was firstly carried out on the GaP substrates using a mixture of $HF/KMnO_4$ solution with different concentrations. By using the same etching conditions, GaP nanowires were successfully fabricated from the epilayers.

GaP/Si heterojunction nanodiodes were then fabricated using Au-Ge/Ni contacts on the GaP epilayer and Al/Ni on the backside of Si. Transport properties of the nanodiode array confirmed the possibility of using the array as a low-noise electronic device.

Zusammenfassung

Seit Jahrzehnten wird an der Integration von III-V Halbleitern auf Silizium gearbeitet. Dieses Ziel scheint erreichbar zu sein, allerdings gibt es dabei noch viele Herausforderungen wie beispielsweise verschiedene Kristalldefekte. Dass Defekte, beispielsweise Versetzungen, trotz der geringen Gitterfehlanpassung von GaP und Si auftreten, ist mit dem großen Unterschied des thermischen Expansionskoeffizienten der beiden Materialien zu erklären.

In dieser Arbeit wird das epitaktische Wachstum von GaP/Si Heterostrukturen zur Herstellung von rauscharmen GaP/Si Nanodiodenarrays untersucht, wobei eine top-down Ätztechnik zur Herstellung der verwendeten Nanodiodenarrays genutzt wurde. Zur Untersuchung der gewachsenen Schichten wurden Röntgenstreuung (XRD), Rasterelektronenmikroskopie sowie die elektrische Charakterisierung mittels Strom-Spannungs und Kapazität-Spannungsmessungen verwendet. Zudem wurde die Grenzfläche zwischen epitaktischer Schicht und Substrat mittels Niederfrequenter Rauschspektroskopie (LFN) untersucht.

Die GaP-Schichten wurden auf p-dotierten Si (100) Substraten mittels eines Riber-32P Gasquellen-Molekularstrahlepitaxiesystems gewachsen. Die Abhängigkeit der Oberflächenbeschaffenheit und Kristallqualität von den Wachstumsbedingungen, wie der Wachstumstemperatur, wurden intensiv untersucht, um die Defektdichte zu minimieren. Dafür wurden nominal 500 nm dicke Heterostrukturschichten bei Wachstumstemperaturen von 550 °C, 400 °C und 250 °C gewachsen, wobei 400 °C als die optimale Wachstumstemperatur bestimmt wurde. Trotzdem waren die erhaltenen Schichten aufgrund der hohen Versetzungsdichte von schlechter Qualität. Eine nur sehr geringe Qualitätsverbesserung konnte durch einen in situ durchgeführten thermischen Annealingschritt bei 500 °C für 10 Minuten erreicht werden. Daher wurde eine neue Annealingmethode vorgeschlagen, die in dieser Arbeit step-graded annealing (SGA) genannt wird. Bei dieser Methode wurde die Temperatur schrittweise von 400 °C auf 480 °C innerhalb von 90 Minuten erhöht. Dabei wurde die Oberfläche die gesamte Zeit mittels Reflexion hochenergetischer Elektronen (RHEED) untersucht. Die Oberflächenrekonstruktion, die während des Annealens mittels RHEED

beobachtet wurde, zeigte schließlich eine große Verbesserung der Kristallqualität. Die Gitterparameter von GaP wurden mittels asymmetrischer XRD gemessen, wobei festgestellt wurde, dass sie exakt denen von Volumen-GaP entsprechen. Zudem wurde festgestellt, dass die GaP-Schicht automatisch n-dotiert ist und diodentypisches Gleichrichtungsverhalten aufweist.

Interessante Informationen über Fallenzustände in den Heterostrukturfilmen konnten mittels LFN-Messungen gefunden werden. In einer nicht annealten Probe wurden beispielsweise zwei Fallenzustände im Bereich der Bandlücke festgestellt. In den mittels der SGA-Methode annealten Proben wurde hingegen ein rauscharmes und fallenfreies System erhalten.

Anschließend wurde Elektronenstrahllithografie (EBL) zum Erstellen von Nanomustern auf der Oberfläche genutzt, die zur Herstellung von Nanodrähten genutzt werden sollen. Zur Optimierung der Elektronenstrahllithografie wurden dabei GaP-Substrate aufgrund der im Vergleich zu den epitaktischen Schichten besseren und glatteren Oberflächenstruktur genutzt. Dabei konnten in einer Goldschicht 200 nm große Löcher in einem Gitter mit hoher Dichte auf GaP erstellt und in die GaP-Schicht übertragen werden.

Die metallunterstütztes chemisches Ätzen (MacEtch) genannte Technik wurde kürzlich vorgeschlagen und eignet sich für die Herstellung von Nanodrähten. Die Anwendung zur Herstellung von Nanodrähten aus GaP war herausfordernd aufgrund bisher begrenzter Anwendung für III-V Halbleiter. Zur Optimierung der MacEtch Technik wurde zunächst wieder GaP-Substrat verwendet, um den Einfluss von Kristalldefekten und der Oberflächenrauigkeit auf die Ergebnisse zu minimieren. Genutzt wurde ein Gemisch aus Lösungen von $HF/KMnO_4$ mit verschiedenen Konzentrationen. Mit den so bestimmten Prozessbedingungen konnten erfolgreich GaP Nanodrähte aus GaP-Epilayern hergestellt werden.

GaP/Si Heteroübergangsnanodioden wurden anschließend unter Nutzung von Au-Ge/Ni Kontakten zu GaP-Schicht und Al/Ni Kontakten zum rückseitigen Si hergestellt. Die Transporteigenschaften des Nanodiodenarrays bestätigen die Möglichkeit, diese Arrays als elektronische NiederLärmbauelemente einzusetzen.

Publications and Conferences

Parts of this work were already been published in the scientific journals and the annual conferences, while other is in progress:

Publications

- **Emad. H. Hussein**, S. Dadgostar, F. Hatami, and W. T. Masselink,
  Thermal annealing effect on the structural properties of epitaxial growth of GaP on Si substrate,
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  J. Cryst. Growth, 425: 94-98, 2015.

- **Emad. H. Hussein**, F. Hatami, and W. T. Masselink,
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Not Related to the Thesis

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- **Emad**. **H**. **Hussein**, F. Hatami, and W. T. Masselink,
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  Low-frequency noise characterization of epitaxial GaP/Si heterostructure,
  E − MRS Conf., Warsaw-Poland, (J-37) P. 172, 15-19 September 2014.

- **Emad**. **H**. **Hussein**, V. Hortelano, M. P. Semtsiv, and W. T. Masselink,
  Fabrication of nanopattern arrays of gold dots for nanowire arrays on GaP substrates by electron-beam lithography,
  DPG Conf., Berlin-Germany, 15 - 20 March 2015.

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CHAPTER-1

Introduction

Introduction

Introduction

The integration between III-V compound semiconductors and silicon (Si) is still a challenge, due to various crystalline defects formed in the heterostructures. Anyhow, many efforts have been made to fabricate high-crystalline quality silicon-based III-V compound devices. One feature of Si is that the economic perspective of using low cost material, thanks to its good physical properties. The III-V compounds are prominent with high cost, while they are very distinctive as high performance materials. Therefore, such integration makes possible to fabricate large-area, high-performance and low-cost devices. For instance, the heterostructure of gallium phosphide (GaP) on Si serves the fabrication of efficient solar cells [Bec-88, Lan-13]. Although growth of GaP on Si was relatively reported by different groups [Mal-82, Suz-91, Tak-98, Doe-08, Doe-11], to the best of our knowledge, a very few studies have adopted the effect of the interface defects on the heterostructure transport properties [Pal-13]. Hence, this issue is deeply discussed in this thesis as a step towards low-noise GaP/Si devices.

1.1 Motivation of Growth of GaP/Si

Various applications have been introduced adopting GaP as a principle material. For instance, GaP microporous showed a good aspect as a photocathode material for solar water splitting cells [Wal-10]. In addition, the GaP/Si heterostructure has recently been investigated for the fabrication of tandem solar cells [Kot-14], which may open the route for the growth of other III-V materials on Si. Hence, with the highly mature technology of Si fabrication, Si-based electronic, optoelectronic and photonic devices have much grown due to its outstanding performance and relatively cheap [Tsc-10, Wan-011].

Regarding III-V compounds, three types of substrates are available: gallium arsenide (GaAs), indium phosphide (InP) and GaP. While GaAs and InP have the ability to achieve high-mobility applications, GaP serves high-temperature applications, because it has the widest bandgap energy (2.26 eV at room temperature). On the other hand, the leakage current is a significant factor that limits the performance of semiconductor devices. As the leakage current is a function of intrinsic carriers, which are very low in GaP, it is reasonable to expect that the leakage current in GaP becomes low relative to Si. That means, the noise generated in GaP-based devices might be lower than that formed by Si-based devices.

In this work, GaP was chosen as a III-V semiconductor material for the growth process on Si substrate due to some features. First, the small lattice mismatch between GaP and Si (∼0.37% at room temperature) qualifies this material to be the most candidates for the growth of III-V compounds on Si. Second, the high-

quality GaP layer could act a superior buffer layer for the integration of other III-V materials on Si [Vol-11]. Finally, due to its wide bandgap and low-intrinsic carriers [Che-07], GaP is expected to show lower noise than the other III-V compounds and Si. However, GaP demonstrates good stability for high-temperature electronics [Zip-82, Sob-98]. Nevertheless, GaP nanowires are not widely used for the fabrication of electronic devices in spite of their good electrical properties in nanoelectronics [Kim-04, Kim-05].

The metal-assisted chemical etching technique is found to be powerful for etching Si nanowires. However, this method is still not familiar in the III-V compounds, and limited to the fabrication of GaAs [DeJ-11] and InP [Kim-15] nanostructures. Regarding GaP, there exists a very recent study of MacEtch of GaP nanocones of height less than 200 nm using a palladium layer [Kim-16]. Therefore, fabrication of GaP nanowires by this technique, using a thin gold layer as a catalyst, was setting a large challenge.

1.2 The Research Objectives

This research involves epitaxial growth and characterization of GaP on Si substrate for the fabrication of low-noise heterojunction-nanodiode array based on GaP nanowires. Since the nanodiode array is the aim of this thesis, the specific objectives comprise the following:

1. Epitaxial growth of GaP on Si substrate using gas-source molecular-beam epitaxy (GSMBE) technique.

2. Design and fabrication of gold patterns on the grown films using electron-beam nanolithography.

3. MacEtch of GaP for the fabrication of vertical nanowires.

4. Fabrication of nanodiode array for low-noise electronic applications.

1.3 Approach

GaP layers were grown on Si substrates using GSMBE technique. The most significant parameters that play a crucial role in the quality of the grown films are the growth temperature and the layer thickness. At a thickness of about 500 nm and growth temperature of 400 °C, the growth conditions were optimized. Since the crystal quality of the epilayers was found to be poor at these conditions, the heterostructure films in situ was thermally annealed using a new approach at which the temperature was raised slowly to 480 °C for 90 min. During the annealing, the

GaP layer was monitored by RHEED. At the end of annealing, the crystal quality was highly improved, and found to be n-type auto-doped.

GaP substrates and the GaP epilayers were coated with an electron-beam (e-beam) resist, called Polymethyl methacrylate (PMMA), for printing nanolithographic patterns on the resist. Upon the printed pattern, a gold layer of thickness of 25 nm was evaporated. After lifting-off the unwanted metal, nanopattern of gold layer was transferred to the GaP substrates. Similarly, nanopatterns of gold were successfully made on the GaP epilayers. Then, fabrication of GaP nanowires from the epilayer was carried out using MacEtch method by dipping the sample in a mixture of $HF/KMnO_4$. After evaporating gold-germanium/nickel contact on the nanowires and aluminium/nickel contact on the backside of Si, GaP/Si heterojunction nanodiodes were fabricated. Electrical properties of the nanodiodes and the LFN spectra confirm the applicability of the device for low-noise electronics.

1.4 Thesis Outline

In this thesis, growth of GaP/Si heterostructure and fabrication of nanodiode array based on nanowires are reported. The thesis structure consists of the following chapters:

- **Chapter 1** presents an introduction to the research project, motivation of growth GaP on Si, challenges associated to the nanostructures fabrication, objectives of the research and thesis approach.

- **Chapter 2** reviews the theoretical concepts of heterostructures, taking into consideration a survey of literature published in this field.

- **Chapter 3** demonstrates the theoretical concepts of e-beam lithography as well as the theory of semiconductor etching for nanowire fabrication.

- **Chapter 4** describes the characterization methods and tools used for analyzing the results.

- **Chapter 5** reports the experiments of growth of GaP/Si heterostructures using GSMBE. The analyses of the grown layers, using different characterization tools, are also discussed in this chapter.

- **Chapter 6** focuses on the fabrication of EBL nanopatterns on GaP substrates and GaP/Si films. SEM images for the lithographic patterns and optimization of printing process are displayed. Thereafter, fabrication of nanowire diodes by using MacEtch process and finally fabrication of nanodiode array are reported and then analyzed.

- **Chapter 7** summarizes the work presented in this thesis, including conclusion of the results. It also discusses the future work related to epitaxial GaP/Si nanostructure applications.

CHAPTER-2

Review of Semiconductor Heterostructures

Review of Semiconductor Heterostructures

Introduction

The main challenge in electronic devices that fabricated from two, or more, different semiconductor materials is the growth of high-quality heterostructure films with as low crystalline defects as possible . Many defects in the grown layer present due to difference in their physical properties. This chapter summarizes some theoretical topics related to the epitaxial growth of GaP on Si substrate.

2.1 Molecular Beam Epitaxy

The term epitaxy is of Greek root, where (epi) means "***above***" and (taxis) means "***in order manner***". The epitaxial thus refers to arrange monolayers upon a substrate or another material (monolayer: a single atomic or molecular layer). Molecular beam epitaxy (MBE) is a technique used for the epitaxial growth of high quality film on a heated substrate [Plo-81]. The MBE growth process is based on evaporation of molecular or atomic beams and then directed to a substrate under ultra-high vacuum environment, which is about 10^{-8} Torr. Epitaxial films may either be homoepitaxial [Bai-90], in which all films are grown on a substrate with the same materials, or heteroepitaxial [Bol-09] when the films and the substrate have different materials. The aspect of MBE is the ability to achieve growth of materials at low temperature and low growth rate.

2.1.1 Gas-Source Molecular-Beam Epitaxy

Various types of MBE systems are currently available for epitaxial growth. Among them are gas-source molecular-beam epitaxy, solid- source molecular-beam epitaxy (SSMBE), plasma-assisted molecular-beam epitaxy and metal-organic vapour-phase epitaxy (MOVPE). Different semiconductor materials can be grown using these systems. The work presented in this thesis is limited to GSMBE, whose photo is shown in Fig. 2.1. This system consists of two ultra-high vacuum chambers: load-lock chamber and growth chamber. Each chamber can be pumped independently by ionic and turbo pumps, respectively. The sample is transported between the chambers using a manipulator rod, keeping the vacuum state unchanged. While the manipulator catch the sample holder, it is possible to rotate it around its axis to mount the holder in its position. Thermally cleaning the substrate is firstly achieved in the load-lock chamber at about temperature of 200 °C before transferring to the growth chamber. Cooling the chambers is achieved by passing liquid nitrogen in cryopanels surround the main internal chamber wall. The cryopanels enable thermal isolation among the material cells.

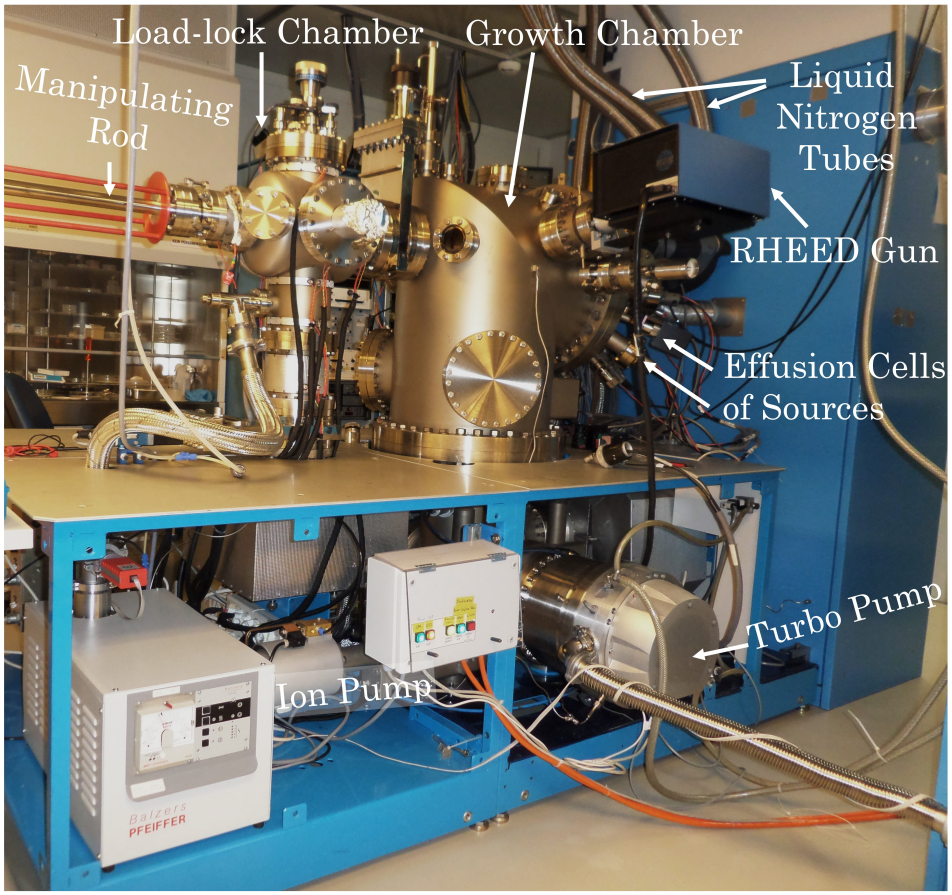

Figure 2.1: *Photograph for the ISA-Riber-32P gas-source MBE that was used for the growth experiments (FET group/Humboldt-University in Berlin). The system consists of load-lock chamber, growth chamber, manipulator rod for transferring the sample holder between the chambers, effusion cells for source materials, RHEED gun, ion pump and turbo pump. The system can be cooled by flowing liquid nitrogen through the inner wall of the growth chamber.*

Figure 2.2 illustrates a scheme of a typical MBE growth chamber. In this chamber, the substrate holder is mounted on a movable stage that can be adjusted to face the source beams. The substrate is heated by a heater in the stage, and the temperature can be controlled by an external power supply and measured by a calibrated infrared optical pyrometer. This system is equipped by a RHEED gun, which is biased by a voltage between 6 and 8 kV. For the growth of III-V semiconductor compounds, a number of effusion cells are attached to the growth chamber. Each cell contains a crucible made of pyrolitic boron nitride, and heated by a filament to high temperatures. In front of the cell, a mechanical shutter is mounted to switch on / off the material beam.

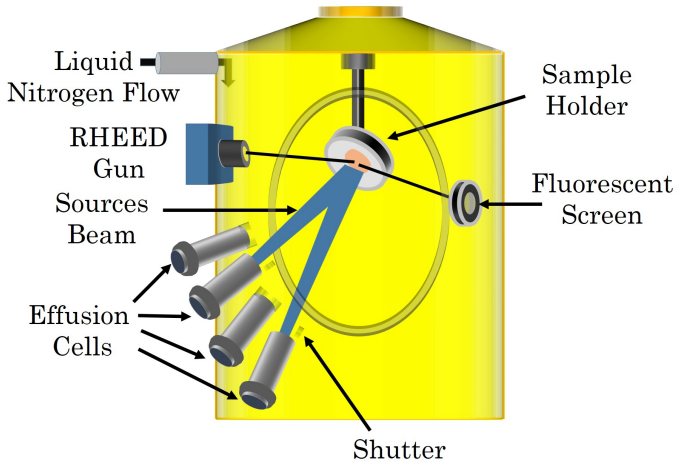

Figure 2.2: *Scheme of typical MBE growth chamber. It consists of a number of effusion cells that can be used for different materials evaporation, and RHEED gun, which is used for monitoring the growth progress. The chamber is cooled by liquid nitrogen flow in the inner wall.*

In the GSMBE system used in this research, type III materials include gallium (Ga), indium (In) and aluminium (Al). These solid materials can be evaporated in the crucibles of the effusion cells at different temperatures using external power supplies. The type V elements are arsenic (As) and phosphorus (P) cracked from arsine gas (AsH_3) and phosphine gas (PH_3) at temperatures from 830 to 850 °C. In addition, the MBE system has two effusion cells of Si and beryllium (Be) used for n and $p-type$ doping, respectively. The growth process in MBE is controlled by a computer as well.

An aspect of MBE growth system is the growth rate that can be controlled such that the number of monolayers per time of growth can be determined. The number of molecules G colliding the substrate per unit area in second is expressed by [Man-05]:

$$G = 3.513 \times 10^{22} \frac{AP}{\pi\, l^2 \sqrt{MT}} \qquad molecules\ per\ (cm^2.s), \tag{2.1}$$

where A, P, l, M and T are the area of the source material aperture, source vapour pressure, distance between the substrate and the sources, molecular weight and temperature, respectively. Thus, the number of the atoms striking the surface is mainly dependent on the pressure and temperature of the source cells in addition to the instrument parameters. With knowing all these parameters, G is calculated and then the growth rate can be calculated by dividing G on the number of atoms of the source per unit area, e.g. GaAs has 6.258×10^{14} atoms/cm^{2}s.

Under the ultra-high vacuum of the MBE system, the growth surface is relatively kept clean against contamination, which may cause undesirable effects in the

properties of the growth films. Hence, one advantage of a load-lock chamber is to isolate the growth chamber from contamination at the atmosphere during loading the sample [Art-02]. The growth chamber is also equipped with a mass spectrum analyzer (MSA), which detects different vapours and consequent has an advantage of detect problems with the vacuum, such as residual gases in the chamber.

2.2 Theory of Heterostructure

In semiconductor, the term of heterostructure refers to any system made of two, or more, different semiconductor materials. The materials are always different in their energy bandgaps, and usually in lattice constants. The major problem is the growth of heteroepitaxial materials with minimum crystalline defects. For instance, strain in the epilayer is regarded a reason for dislocations formation in the interface. Hence, this issue has intensively been investigated in growth of III-V materials on Si substrate [Bol-09]. Once a lattice-mismatched epilayer is grown on a substrate (or underling layer), the surface layer is initially constrained (or expanded) so that the horizontal lattice parameter matches that of the substrate. This case is continued as long as the epilayer thickness (h) does not access a certain value called a critical thickness (h_c). When the layer thickness increases, the strain energy increases. Beyond critical thickness dislocations are formed [Tak-10] and therefore, it is energetically favourable to relax the strain in order to reduce the strain energy.

Although GaP has small lattice mismatch with Si, which is $\sim 0.37\%$ at room temperature, the large difference in their thermal expansion coefficients and growth of polar on non-polar material cause a generation of various crystalline defects [Bac-96, Kum-11]. In general, defects like dislocations, stacking faults, antiphase domain, etc. have been investigated by several groups using different growth techniques [Tak-98, Ohl-02, Kun-08, Yam-09, Lin-13].

A schematic representation for heteroepitaxial layers, with different lattice parameters, grown on a same type of substrate is shown in Fig. 2.3. A lattice-matched layer can be grown, when both the layer and substrate have approximately the same lattice constants (Fig. 2.3(a)), without thermal expansion mismatch. An example of such case is the growth of AlGaAs layer on GaAs substrate [Sat-90]. In contrast, growth of an epilayer with bigger lattice parameter than that of the substrate is shown in Fig. 2.3(b). If the layer is very thin, it will be constrained so that the parallel lattice parameter coincides with that of the substrate, while the perpendicular lattice parameter increases. The misfit between the epilayer and the substrate is accommodated by a tetragonal distortion, so the layer experiences an elastic strain. In this case, the layer is referred to as a coherent strained-layer. Also, an inverted attitude, shown in Fig. 2.3(c), may occur when the layer has smaller lattice parameter than that of the substrate, where the layer expands horizontally and shrinks

perpendicularly. However, as Fig. 2.3(d) shows, when the thickness of the strained layer increases, the strain will relax by producing dislocations at the interface.

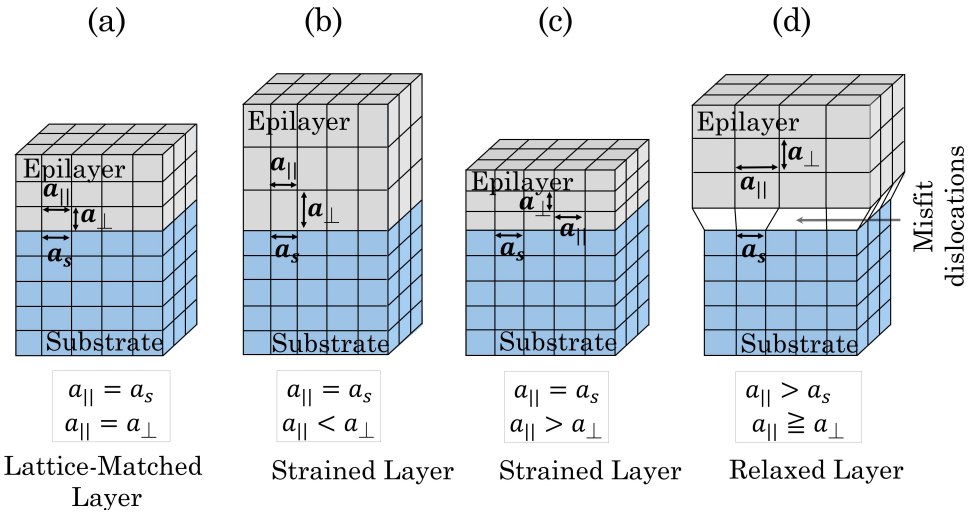

Figure 2.3: *Schematic representation of epitaxial growth of (a) lattice-matched epilayer on a substrate, (b) coherent-strained lattice-mismatched epilayer on a substrate of a smaller lattice parameter, (c) coherent-strained lattice-mismatched epilayer on a substrate of a bigger lattice parameter and (d) relaxed lattice-mismatched epilayer on a substrate of a smaller lattice parameter.*

2.2.1 Strain and Relaxation

The room-temperature lattice mismatch between a layer of lattice parameter a_l and a thick substrate of lattice parameter a_s can be measured by the misfit strain given by:

$$\varepsilon_\circ = \frac{a_l}{a_s} - 1, \tag{2.2}$$

Consider the growth of a cubic-lattice layer on a cubic-lattice substrate, such as GaP/Si, produces a coherent strained-layer. The in-plane lattice parameters of the layer, that are parallel to the interface, will be $a_l = b_l$, and denoted by $a_\parallel$, and the out-of-plane parameter perpendicular to the substrate will be c_l, and denoted by $a_\perp$. The perpendicular and parallel lattice mismatch, $m_\perp$ and $m_\parallel$ respectively, are given by:

$$m_\perp = \frac{a_\perp}{a_s} - 1, \tag{2.3a}$$

$$m_\parallel = \frac{a_\parallel}{a_s} - 1. \tag{2.3b}$$

Substituting Bragg's law ($\lambda = 2d \sin\theta_s$) into Eq. 2.3a yields

$$a_\perp = a_s \left(\frac{\sin(\theta_s)}{\sin(\theta_s + \Delta\theta)} \right), \tag{2.4}$$

where θ_s is the Bragg's angle of the substrate and $\Delta\theta$ is the XRD peaks splitting between the substrate and the layer, where $\Delta\theta = \theta_L - \theta_s$ with θ_L being the Bragg's angle of the layer. The perpendicular lattice strain of the layer $\varepsilon_\perp$ is calculated by:

$$\varepsilon_\perp = \frac{a_\perp}{a_L} - 1, \tag{2.5}$$

where a_L is unstrained lattice parameter of the layer (Bulk). This strain has either positive value, if the layer is extensive, or negative value, when it is shrunk. On the other hand, the residual strain of the layer in the direction parallel to the substrate can be calculated by:

$$\varepsilon_\parallel = \frac{a_\parallel}{a_L} - 1. \tag{2.6}$$

Then, the relaxation degree of the epilayer can be given as [Bir-06]:

$$R(\%) = \frac{a_\parallel - a_s}{a_L - a_s} \times 100, \tag{2.7}$$

which ranging from R = 0, for the fully strained layer, to R = 1 for the fully relaxed layer.

2.2.2 Critical Thickness

As has been mentioned above, the strain energy increases when the thickness of epitaxial layer exceeds the critical thickness. The idea of the critical layer thickness is based on the fact that below which the layer is coherently strained with no interfacial dislocations, while above which the generation of misfit dislocations is energetically favourable. An approach for the critical thickness calculation was developed by Mere in 1963 [Mer-63]. It was considered that beyond critical thickness the reduction of the elastic strain energy (E_S) of the epilayer may equal to the total energy of the interfacial dislocations (E_D). In the most cases, the layer is thicker than h_c, so the misfit dislocations at the heterostructure interface are introduced to relieve the elastic strain. As a result, there will be two forces at the interface: the force due to the misfit strain and the force of the dislocations. The thickness is regarded a critical thickness, when the forces are balanced. Thus, the total strain energy in the system will be:

$$E_T = E_S + E_D, \tag{2.8}$$

But if the misfit strain force is bigger than the force of dislocations, with the increase of the film thickness, dislocations will move to reduce E_T causing relaxation the layer [Mat-74].

Determination of the critical thickness was already been intensively investigated by many researchers [Koh-88, Ana-92, Kim-06, Har-11]. Furthermore, a number of models have been proposed to estimate the critical thickness of the strained epilayer. For example, Matthews and Blakeslee proposed a model for calculating the critical thickness of GaAs-$GaAs_{0.5}P_{0.5}$ on GaAs substrate [Mat-74]:

$$h_c = \frac{b}{4\pi f}\frac{1-\nu cos^2\theta}{1+\nu cos\lambda}\left(\ln\frac{h_c}{b}+1\right), \tag{2.9}$$

where θ and λ are 60° for diamond and zinc blende crystals. For a single epilayer, this equation is multiplied by a factor of 1/4.

Later, People and Bean [Peo-85] calculated the critical thickness of Ge_xSi_{1-x}/Si for $0 \leq x \leq 1$. In this model, it was assumed that at the critical thickness the misfit dislocation at the interface is formed when the areal strain energy density of the film becomes higher than that of an isolated screw dislocation. However, in both models, the value of h_c is inversely dependent on the misfit strain.

2.2.3 Polar on Nonpolar Epitaxy

One of the most essential issues of epitaxial GaP/Si is the growth of a polar on a nonpolar material. Silicon consists of identical atomic species attached to each others by covalent chemical bonds. Hence, the net electric dipole is zero and the material is then called a nonpolar. In contrast, GaP is combined from Ga and P atoms attached by ionic bonds having electric dipoles, resulting in a polar crystal. According to Harrison et al. model [Har-78] a large electric charge is induced in the interface between the GaP layer and the surface of Si. Therefore, some atoms will move in order to neutralize the charge causing defects in the interface or/and in the GaP layer.

2.2.4 Thermal Strain

A significant parameter of the material thermal properties, which plays an important role in determination of strain relaxation in the layer, is the thermal expansion coefficient (α). The expansion or contraction of the crystal lattice as the temperature changes is related to difference in the thermal expansion coefficients ($\Delta\alpha$) of the grown materials. If $\Delta\alpha$ is small, both materials can expand and contract at the same rate during heating or cooling to room temperature. In the case of GaP/Si this difference is large, where ($\Delta\alpha = \alpha_{GaP} - \alpha_{Si}$) is equal to 1.96×10^{-6} °C^{-1} at room temperature, with $\alpha_{Si} = 2.6 \times 10^{-6}$ °C^{-1} and $\alpha_{GaP} = 4.56 \times 10^{-6}$ °C^{-1}. At a given growth temperature, this difference increases, which results in a thermal stress in the epilayer. Using Hooke's law for cubic crystal (e.g. GaP) with (001) plan parallel to the substrate, the thermal stress is given by [Pea-91]:

$$\sigma_T = C\Delta\alpha\Delta T, \tag{2.10}$$

where $C = c_{11} + c_{12} + (2c_{12}^2/c_{11})$ with c_{11} and c_{12} are elastic constants of GaP, whose values are equal to 14.05×10^6 N/cm^2 and 6.2×10^6 N/cm^2, respectively. The thermal stress produces a thermal strain in the GaP layer, which is accommodated by a tetragonal distortion in the GaP lattice. The thermal strain is expressed as $\varepsilon_T = \sigma_T/C$, and thereby Eq. 2.10 becomes

$$\varepsilon_T = (\alpha_{GaP} - \alpha_{Si})\ (T_g - T_r), \tag{2.11}$$

where T_g and T_r are the growth and room temperatures.

On the other hand, in order to improve the crystal quality of the epilayer, the film in situ is almost thermally annealed. The thermal annealing mainly affects the strain in the layer. Similarly, when the system temperature is increased from growth temperature to annealing temperature (T_a), the thermal strain will more increase, and thence ε_T can be calculated from Eq. 2.11, taking $\Delta T = T_a - T_g$ into account.

2.3 Heterojunction Energy Band Diagram

Most of electronic and optoelectronic devices are often fabricated using two, or perhaps more, kinds of semiconductor materials forming heterojunction(s) (HJ). A wide range of applications involve HJ, such as heterojunction bipolar transistors (HBTs) [Mit-05, Mar-14], heterostructure field effect transistors [Liu-06] high electron-mobility transistors (HEMTs) [Lee-15], heterojunction nanowire [Lee-07] and etc. In a $p-n$ homojunction, the electrons can diffuse from the n-region to the p-region, and holes can diffuse to the n-region. Without an applied voltage, the conduction and valence band edges will line up, while the Fermi level will be constant at the junction. This mechanism also occurs in HJ in addition to present offset in the badgap edge.

In spite of the widespread use of HJ, few efforts adopted the energy band alignment, especially in GaP/Si HJ [Per-84, Isl-07, Sak-08]. However, a first approach for energy band structure of Ge/GaAs HJ was proposed by Anderson in 1960 [And-60]. Here, we restricted only to two different semiconductor materials, which are p-type and n-type whose energy gaps are E_{g1} and E_{g2}, respectively, where $E_{g1} > E_{g2}$. An example of such system is AlGaAs/GaAs HJ, which is somewhat similar to GaP/Si. The bandgap alignment of such system is then referred to as type-I.

First, we consider these two materials are isolated. Figure 2.4 shows their band alignment, in which the vacuum energy level is the same for both materials. Due to the difference in the energy gaps, the edges of the conduction and valence bands will show discontinuities designated by ΔE_C and ΔE_V, when the materials are attached together. In the Anderson's approach, the values of ΔE_C and ΔE_V are dependent on the electron affinities X_1 and X_2. As the Fermi level of the n-type region is higher than that of the p-type region, the electrons will flow from the n-type region to the

p-type region, and holes will flow in the opposite direction. Since electrons deplete the n-type region, a positive depletion region is made in it. Likewise, a negative depletion layer is formed in the p-type region. These two depletion layers finally lead to bend up the energy bands of the n-type region, and bend down those of the p-type region. Thus, in the equilibrium condition at zero-bias voltage, the Fermi level in both sides will line-up such that it becomes the same for both of them. This case is shown in Fig. 2.4(b).

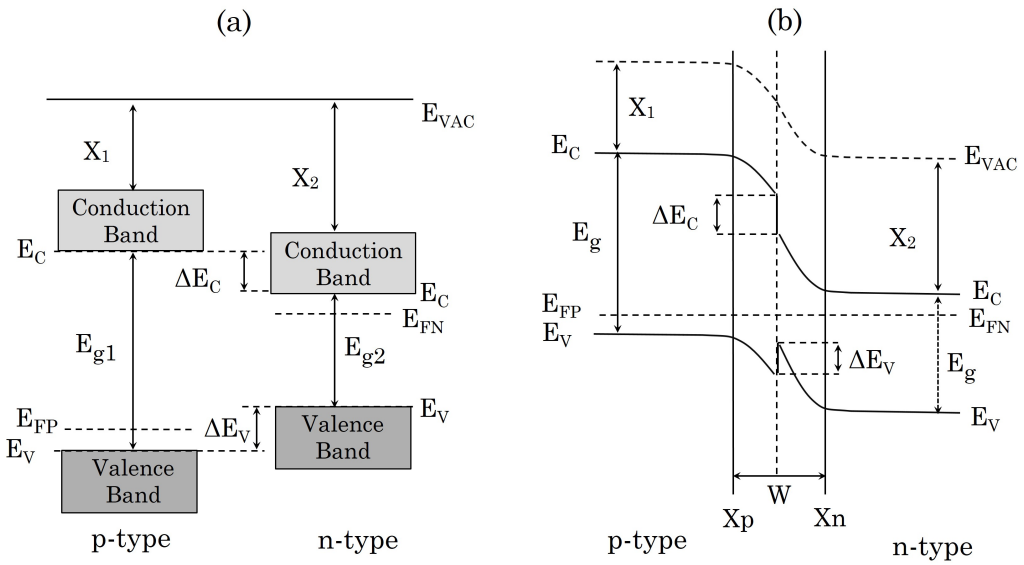

Figure 2.4: *Energy band diagram of a $p-n$ heterojunction diode in thermal equilibrium. (a) Isolated HJ and (b) attached HJ. E_{g1} is the p-type material energy gap, E_{g2} is the n-type material energy gap, E_{FP} and E_{FN} are their Fermi energies, ΔE_C and ΔE_V are the conduction and valence band discontinuities, E_{VAC} is the vacuum energy level. X_1 and X_2 are the affinity of electrons in the p-type and in the n-type material, and W is the heterojunction width.*

In order to extrapolate the HJ parameters, such as the capacitance of HJ, a depletion approximation is taken into consideration. In this approximation, it is assumed that the majority carrier concentration is zero in the two depletion regions, whose thicknesses are X_p and X_n. Thus, on both sides of HJ, the net charge is expressed by:

$$qN_dX_n = qN_aX_p, \tag{2.12}$$

where N_d and N_a are the donor and acceptor carrier densities, respectively. The depletion width (W) is given as:

$$W = X_p + X_n. \tag{2.13}$$

The energy band alignments of a heterojunction diode in the forward bias and reverse bias are shown in Fig. 2.5(a and b), respectively.

When the heterojunction diode is forward biased ($V > 0$), the electric potential across the depletion region will decrease by a mount of V and becomes $V_{bi} - V$. Consequently, the depletion region width will decrease producing the band alignment shown in Fig. 2.5(a). In this case, the difference between their Fermi levels is equal to qV_{bi}. As Fig. 2.5(b) shows, if HJ is reversed biased ($V < 0$), the depletion region width increases and the band diagram will then change. Thence, the difference between their Fermi levels is equal to $-qV_{bi}$.

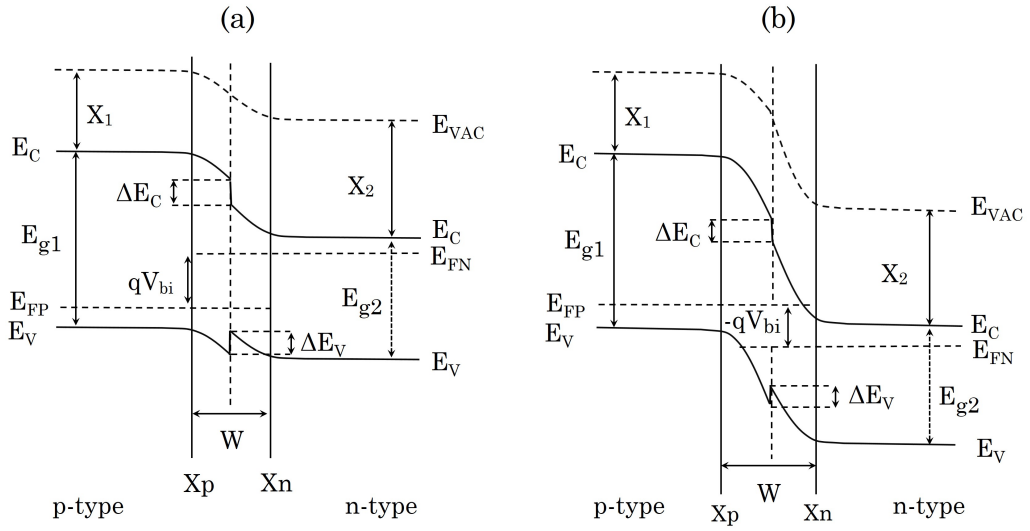

Figure 2.5: *Energy band diagram of a $p-n$ heterojunction diode in forward bias (a) and in reverse bias (b). E_{g1} is the p-type material energy gap, E_{g2} is the n-type material energy gap, E_{FP} and E_{FN} are their Fermi energies, ΔE_C and ΔE_V are the conduction and valence band discontinuities, E_{VAC} is the vacuum energy level. X_1 and X_2 are the affinity of electrons in the p-type and in the n-type material, and W is the heterojunction width.*

2.4 Low-Frequency Noise Spectroscopy

The output voltage of an electronic device is usually accompanied with a random fluctuation causing a distortion in the output signal shape. The fluctuation is referred to as an electronic noise. Accordingly, performance of the device is affected by the noise, especially when its level becomes comparable with the device output. Although the noise is undesirable, low-frequency noise (LFN) spectroscopy is a reliable technique used to investigate the crystalline quality and transport properties of semiconductors.

LFN in electronic devices has gained a large area in the researches for long time

[Rhe-87, Jan-93, Ke-08, Mou-10, Bon-11, Xie-14]. The noise is classified into two kinds: external and internal noise. The external noise is caused by electromagnetic fields issued from the mechanical and electronic instruments, such as electric pumps. The second kind of the noise is generated in the semiconductor devices due to physical origins, like defects formed in the structures. Although, the noise cannot be completely diminished, miniature its effect allows improving the performance of the devices. Therefore, the main objective of the LFN measurements is to figure out the origin of the noise so that it is possible to decrease its levels. Regarding our study, three types of LFN in heterostructure are almost investigated. These are white noise that consists of thermal and shot noises, generation-recombination $(G-R)$ noise and flicker or $(1/f)$ noise.

2.4.1 Thermal Noise

Thermal noise, or so called Johnson-Nyquist noise, arises in the resistance of material. Due to collisions of charge carriers in the material with phonons, the electrons exhibit Brownian motion with a kinetic energy proportional to temperature of the system. The random motion of electrons gives rise to voltage fluctuations. Then, the thermal voltage spectral density of a resistance (R) measured at temperature (T) and frequency bandwidth (Δf) is given by:

$$S_V = 4kTR, \tag{2.14}$$

where $S_V = V^2/\Delta f$, with V being the thermal noise voltage across the resistor, k is Boltzmann constant. Likewise, the thermal current noise spectral density is expressed as:

$$S_I = \frac{4kT}{R}, \tag{2.15}$$

where $S_I = I^2/\Delta f$, with I being the thermal noise current passing through the resistor. The thermal noise is a white noise because its value is independent of frequency.

2.4.2 Shot Noise

In accordance with the Schottky's theory of shot noise in vacuum tube, the direct current passing through a semiconductor junction is almost accompanied with shot noise. Hence, it takes place when the electrons across the potential barrier of a junction, such as a Schottky-barrier diode, a $p-n$ junction diode or a bipolar junction transistor. The shot noise spectral density is given as [Bee-92]:

$$S_I = 2qI, \tag{2.16}$$

where I is the forward bias current passing through the junction and q is the electron charge. The shot noise is usually frequency independent, and hence it is called a white noise.

2.4.3 Generation-Recombination Noise

This type of the noise is produced due to fluctuation in the number of free electrons, which consequently causes a resistance fluctuation. During wafer processing, carrier traps can be formed due to the existence of contaminated elements, such as carbon atoms. Additionally, traps in a semiconductor device is generated during growth process. The traps are electronic-state levels within the energy gap. Hence, electrons from the conduction band, or valence band, can be trapped or de-trapped by these levels. Besides trapping or releasing electrons from the traps, the $G-R$ noise process is also possible via generation or recombination of electron-hole pair. Such events produce a fluctuation in the total voltage or current. Thereby, the number of electrons is fluctuated as a result of $G-R$ process. The spectral density of number of $G-R$ noise processes is given by:

$$S_I(f) = \sum_i \frac{B_i \; I^2}{1 \; + \; (f/f_i)^2}, \tag{2.17}$$

where B_i is a certain $G-R$ noise amplitude that corresponds to its corner frequency of the trap (f_i).

2.4.4 Flicker Noise

Flicker noise is a low-frequency noise, whose spectrum is inversely proportional to the frequency, and therefore it is usually called $1/f$. The origin of the noise is still not fully understood. It is thought that flicker noise may be caused by contacts resistance [Che-94] or surface recombination [Dil-79]. However, the $1/f$ noise was interpreted as a fluctuation in the conductance (ΔG) of a homogeneous semiconductor and formulated in an empirical relation by Hooge [Hoo-69, Hoo-72]:

$$\frac{\Delta G}{G^2} = \frac{\alpha_H}{N}\frac{\Delta f}{f}, \tag{2.18}$$

where G, α_H and N are the sample conductance, a dimensionless constant called Hooge factor and the total number of free charge carriers, respectively. The ratio of $(\Delta G/\Delta f)$ is referred to as the conductance fluctuation density. The fluctuations of conductance are practically measured by current fluctuations ($S_I(f)$) or voltage fluctuations ($S_V(f)$), and thence Eq 2.18 is given by [Hoo-81]:

$$\frac{S_I(f)}{I^2} = \frac{S_V(f)}{V^2} = \frac{\alpha_H}{N}\frac{1}{f^\gamma}. \tag{2.19}$$

In general, $S_I(f)$ (or $S_V(f)$) is also called noise current (or noise voltage) spectral density. The amplitude of flicker noise ($A_{1/f}$) is expressed as:

$$A_{1/f} = \frac{\alpha_H}{N}. \tag{2.20}$$

It was well-established, from the experiments conducted on $1/f$ noise, that the exponent γ is almost one, or very close to unity with a bit deviation of ($\pm$ 0.1). On the other hand, the value of α_H was first proposed to be constant of 2×10^{-3} for semiconductors and metals [Hoo-72]. Later, it was found that this parameter is not constant, but each material has an individual value. For instance, the Hooge factor of n-type GaP was calculated to be 9×10^{-3}, whereas it was equal to 6×10^{-3} for n-type GaAs [Van-74]. Furthermore, this factor depends on the crystalline quality of material. For example, α_H of B-doped diamond varies from 10^{-3} for high quality film to 4×10^{-1} for poor quality film [Che-98].

The electric conductivity in a semiconductor, whose concentrations of free electrons and holes are n and p, is given as:

$$\sigma = q\ (\mu_n\ n + \mu_p\ p), \tag{2.21}$$

where q, μ_n and μ_p are the elementary charge, the electron and hole mobilities, respectively. Equation 2.21 tells us that the mobility fluctuations or the carrier number fluctuations could lead to the conductance fluctuations. The mobility fluctuations arise due to various scattering mechanisms. By using Matthiessen's rule, the mobility of a semiconductor is given by:

$$\frac{1}{\mu} = \frac{1}{\mu_I} + \frac{1}{\mu_L} + \frac{1}{\mu_S}, \tag{2.22}$$

where μ_I, μ_L and μ_S, respectively, the mobility due to impurities scattering, the mobility due to phonon scattering and the mobility due to surface roughness scattering. From Eq 2.22, the mobility fluctuations can be given by:

$$\Delta\mu = \left(\frac{\mu}{\mu_I}\right)^2 \Delta\mu_I + \left(\frac{\mu}{\mu_L}\right)^2 \Delta\mu_L + \left(\frac{\mu}{\mu_S}\right)^2 \Delta\mu_S. \tag{2.23}$$

According to this equation, the mobility fluctuation increases when the impurities increase and when the charge carriers are scattered by the lattice vibrations, as well as due to fluctuation that is caused by the surface roughness.

Different models have been proposed to introduce an acceptable explanation for flicker noise. Nowadays, the physical origin of $1/f$ noise in a solid or semiconductor is investigated according two principle theories: the McWhorter [McW-57] and Hooge [Hoo-69] models. The McWhorter theory describes $1/f$ noise as a result of free-carrier number fluctuations (Δn). That means the noise is caused by trapping or detrapping electrons, so fluctuations in the carrier concentration would take place

resulting flicker noise. In the Hooge model, $1/f$ noise, produced in a material, is attributed to the charge carrier mobility fluctuations ($\Delta\mu$). This model is an empirical proposal without a physical interpretation for the mobility fluctuations. After presenting those theories, Handel [Han-75, Han-80] proposed a theory of quantum $1/f$ noise, in which the noise is caused by combination of interaction of electrons with photons, electron-hole pairs, phonons, lattice defects and etc. The theory, however, had unclear concepts, likes scattered carriers emit low-frequency photon (1 Hz), which was commented by Vliet [Vli-88].

The $1/f$ noise of MOSFET, was studied by Valenza et al. [Val-11], and interpreted to follow McWhorter model, where the noise was imputed to charge trapping in oxide layer of the transistor. Also, Ioannidis et al. [Ioa-13] have developed a LFN model for load current and the output voltage for CMOS inverters within Δn model.

The mobility fluctuation theory was also supported by Jindal and Ziel [Jin-81] using a model of phonon fluctuation. In their model, the number of phonons fluctuates randomly, and the electrons are scattered by phonons. The phonon population results in $G-R$ noises, which are transferred to mobility fluctuation due to electron-phonon interaction. The superposition of the $G-R$ noises can form $1/f$ spectrum.

The total noise spectrum of a $p-n$ junction diode consists of three components: $1/f$ noise, $G-R$ noise and white noise (shot and thermal noises). These components are illustrated in Fig. 2.6.

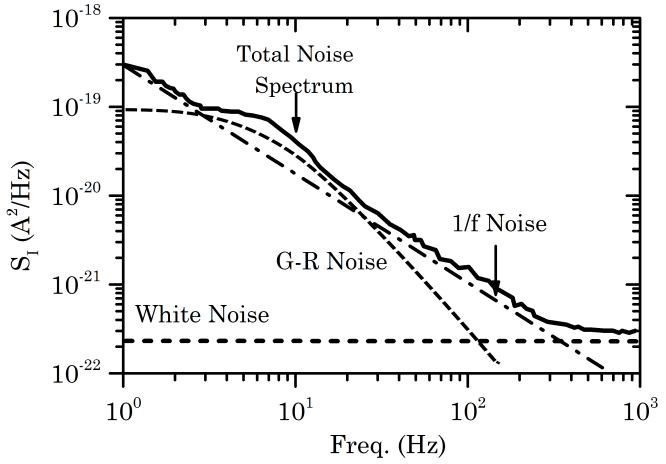

Figure 2.6: *Low-frequency noise spectrum of a $p-n$ junction diode. The total spectrum can be extracted to its components, $1/f$, $G-R$ and white noise.*

The total spectral noise density is thus given by:

$$S_I(f) = \frac{A_{1/f}\ I^2}{f} + \sum_i \frac{B_i\ I^2}{1+(f/f_i)^2} + \left(2qI + \frac{4kT}{R_d}\right), \tag{2.24}$$

where R_d is the junction resistance. It is clear that the flicker noise is linear while the $G - R$ noise is Lorentzian. The white noise has a certain value regardless of frequency change.

2.4.5 Effect of Crystal Quality on LFN

The $1/f$ noise measurement is one tool for characterization of crystalline quality of materials. Vandamme and Oosterhoff investigated the effect of the thermal annealing of a boron-implanted layer in Si on the $1/f$ spectrum [Van-86]. They found that a lower $1/f$ noise was correlated to a better crystalline layer due to annealing, and consequently the Hooge factor was reduced. Also, Chen and Bauhuis [Che-98] studied LFN for diamond of orientation (100) and (110). They found that the Hooge parameter, called noise parameter in the article, for high quality film was reduced as a result of decreasing the impurities. Additionally, the noise spectrum seems to be sensitive to the surface roughness. The relation between the surface roughness and LFN, measured in organic field-effect transistors (OFETs), was reported by Ke at al. [Ke-008]. Their results showed that a much lower noise level in the device corresponds to the lower surface roughness due to reduction of the deep pinholes and the defects by oxygen plasma treatment.

CHAPTER-3

Electron-Beam Lithography and Nanowires

Electron-Beam Lithography and Nanowires

Introduction

Lithography is defined as a process used to transfer a pattern from one medium to another. The ability of using e-beam lithography (EBL) for fabrication of microscale semiconductor devices was familiarized by different groups [Hat-69]. A micrometer pattern was already obtained by spinning a thin layer, called e-beam resist, on a surface and then irradiated by an e-beam. In general, the lithographic pattern is performed by three sequential steps: exposure the resist to an e-beam, development of the written pattern with a suitable chemical solution and finally transferring the pattern to another material. In this chapter, the EBL theory including the interaction of electrons with the resist will be reviewed. Furthermore, fabrication of nanowires by the so called top-down technique using a metallic pattern will be presented.

3.1 Types of Lithography Techniques

Various techniques are utilized for fabrication of lithographic patterns. Each technique has individual parameters that are different from the others, and hence the resolution of the printed patterns are different. This because the nature of chemical and physical interaction of the equipment source with the resist play an important role to determine the pattern resolution. Figure 3.1, presented by Tennant [Ten-99] shows different types of lithography techniques that have been made for obtaining

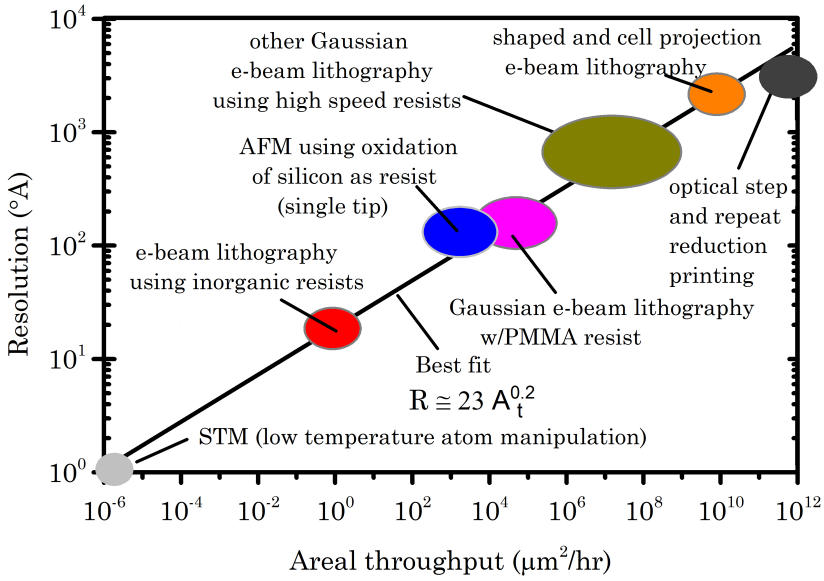

Figure 3.1: *Resolution of a written pattern versus throughput ($\mu m^2/h$) for different lithographic methods. R and A_t are the resolution and the thickness of the resist. Adapted with permission from [Ten-99].*

a high resolution structure with as short time as possible. It can be seen that the faster writing and the least resolution pattern is obtained using optical lithography. Conversely, the slower and the highest resolution is produced by STM technique. However, EBL lies approximately in the middle of these techniques, where high resolution and faster writing than STM or AFM.

3.2 Features and Limitations of EBL

The use of EBL is considered a flexible technique in addition to the possibility of writing complex fashions with sub nanometers patterns. Therefore, for instance, it can be used for the production of masks for other techniques. In contrast, in spite of the EBL features, limitations of the resulting pattern are possibly restricted by the system specifications itself. Among them are the resolution, spot size and the electron source, which determine the brightness and stability of the beam. Moreover, the limitations of EBL are also related to the exposure process, including the chemical properties of the resist and the beam-resist interaction. Hence, the molecular weight of the resist and the exposure doses can strongly limit the resolution of the pattern, especially for a minimum feature size and a maximal density of the written pattern. Concerning to the resist that is required for EBL, PMMA is widely used and considered a good candidate for high resolution e-beam patterns [Gau-11, Gor-11, Gan-14].

However, significant disadvantages relate to the instruments used for EBL writing. For instance, the electron optics of SEM are relatively expensive, as well as EBL is considered a low productivity technique compared to photolithography because of the slow speed writing.

3.3 Electron-Beam Column

The resolution of a written pattern can be evaluated in terms of the shape, separation between two adjacent shapes; e.g. lines or circles, and the feature density [Bro-96]. Whatever the pattern shape or density, the resolution is influenced by the e-beam column shape and the interaction of e-beam with the resist. As illustrated in Fig. 3.2, the e-beam column comprises an electron gun, heated by a tungsten filament source, a number of lenses, aperture, astigmators and blanker. Controlling the intensity, shape and size of the beam can be achieved with these components.

Two types of apertures are typically used in SEM: beam-limiting aperture and blanking aperture. The first one has few holes with different diameters through which the e-beam transfers to the surface. Thus, it is possible to adjust the beam convergence in order to minimize the effect of lens aberrations [Orl-09]. The blanking aperture consists of a pair of parallel plates serves an electrostatic deflector, called

beam blanker. During the scanning process, turning the beam on/off is accomplished by activating the blanker so that it can deflect the beam away from the aperture hole or allow it to reach the surface.

Due to astigmatism arising in the optical components of the SEM system, the e-beam column may be distorted and therefore the position of each point is deflected slightly on the resist, producing an oval pattern instead of a circular one. In the SEM system, the e-beam astigmatism is usually adjusted by an astigmator, which may either be electrostatic or magnetic poles surrounding the optical axis. Finally, in SEM, there are objective lenses can be used for focusing the image on the sample.

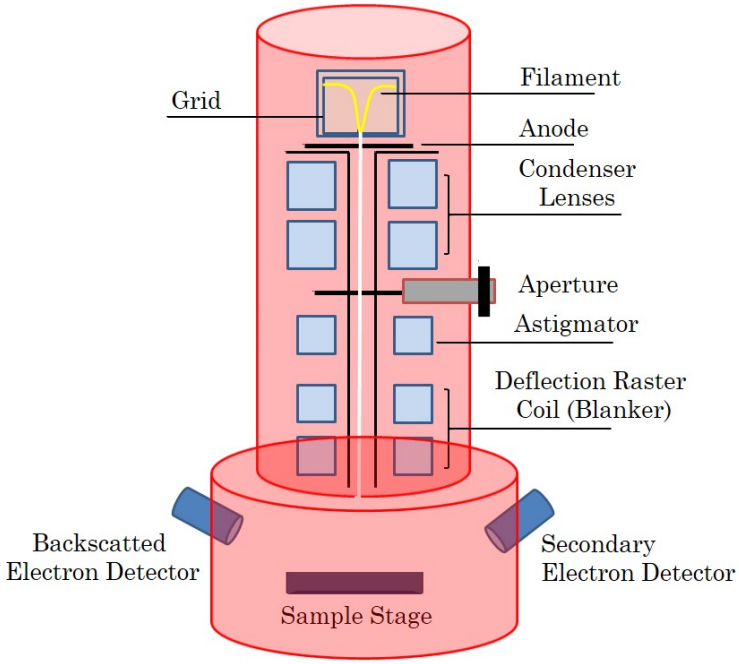

Figure 3.2: *A scheme of the optical elements of the e-beam writing of Jeol JSM6360 system. It is composed of an electron gun, aperture, blanker, astigmator and a number of lenses.*

3.4 Systematic Parameters

The energy of the electron-beam is related to the accelerating voltage of SEM. Consequently, the penetration depth of electrons in the resist depends on the electron energy. At low energy, the e-beam slightly penetrates the resist and the interaction of the beam occurs mainly at the surface. Thus, writing process leads to low resolution and low damage in the resist. At higher energy, the resolution becomes higher, but there is much possibility to increase the damage in the resist structure due to increasing the fragments of the resist or heating the substrate.

As mentioned above, the beam intensity depends on the filament and the beam aperture. The intensity is proportional to the squared radius of the aperture. That is, lower intensity is correlated to smaller aperture which reduces the effect of the beam divergence. Although the smaller aperture is necessary for high resolution, it reduces the image focusing of the SEM and increases the exposure time.

Another parameters that limit the resolution are the image magnification of the SEM and the working distance W_D; the distance between the objective lens and the sample surface. Maximizing the magnification and minimizing W_D give rise to minimize beam deflection respect to the optical axis. The resolution increases, but the working area is decreased. Therefore, for large-area pattern, W_D and M are necessary to be larger.

3.5 Electron-Beam Resist

Nowadays, various types of the EBL resists are available. The available resists are either positive or negative tones. One of the most used resist is PMMA whose chemical formula is $(C_5H_8O_2)n$. It was anciently utilized as high-resolution EBL resist [Hal-68], and recently it is widely used in nanostructures fabrication [Kra-09, Gor-10, Nuz-13, Cui-14]. Its features include high-resolution, high-contrast and non-swelling resist which allows for sub nanometers pattern. But, the main disadvantage of this resist is low sensitivity. The chemical structure of the resist can be altered under the influence of the e-beam radiation. PMMA behaves as a positive or a negative resist during e-beam irradiation. The first demeanour is satisfied at low-energy exposure, where the polymeric bonds are broken making the resist soluble in the developer solvent. Alternatively, when the e-beam energy is high enough, PMMA will lose most of hydrogen and oxygen atoms, causing the exposed region insoluble in the developer [Dua-09].

3.6 Electron-Beam Transport

When an EBL resist is irradiated by an e-beam, its molecular chains are broken leading to reduce the average molecular weight. The EBL resolution is considerably related to the electrons scattered as a result of interaction of the electrons with the resist and the substrate. These electrons cause extra exposures either in the designed area or near it, giving rise to decrease the pattern resolution. Greeneich and Duzer [Gre-74] have introduced a scattering model in which they described that the incoming electrons interact with the resist and penetrate to the substrate. The penetrating electrons experience two major scattering phenomena: forward scattering and backscattering. These types of the electron scattering are mainly dependent on the electron accelerating energy.

The electrons entering the resist experience small-angle elastic collisions with the resist atoms, causing slightly deflect the electrons and subsequently broaden the e-beam. The effective beam diameter (d_f) depends on the accelerating voltage (V_{ac}) and the thickness of the resist (t_r) according to the below empirical formula [Cho-97].

$$d_f = 0.9\ (\frac{t_r}{V_{ac}})^{1.5}, \tag{3.1}$$

With high-energy electrons as well as a thin resist, d_f can be reduced as low as possible. As the divergence of the beam is reduced, distortion in the resolution of the pattern is reduced as well. A fraction of the electrons that penetrate into the substrate exhibit large-angle collisions with the substrate atoms beneath the resist, producing backscattered electrons. These electrons return back to the resist at a certain distance away from the point at which the e-beam is incident. The backscattered electrons expose the resist causing the so called "proximity effect" (see next section).

In addition to the above scattering events, another inelastic interaction that produces secondary electrons is possible. When the primary electrons undergo inelastic collisions with the resist atoms, ionized electrons leave the atoms with low energies and travel only a few nanometers in the resist. The resolution is thereby reduced because these electrons can cause a slight widening of the exposed region.

In the positive EBL resist, there exist three possible configurations of the edge profile of the exposed area, depending on the e-beam energy and the development time. The edge profile at high dose is dominated by the energy of beam regardless of the development time, as shown in Fig. 3.3(a). With a low dose and long development time, the profile is referred to as a V-type (Fig. 3.3(b)). Finally, as shown in Fig. 3.3(c), in the case of medium dose together with the development time, steeper edges can be obtained.

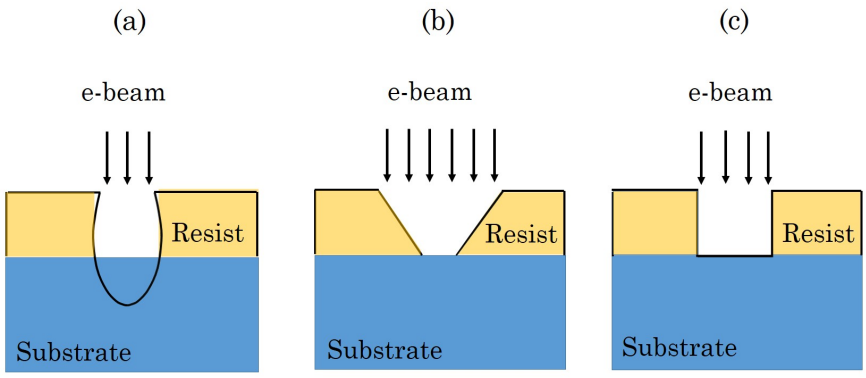

Figure 3.3: *Configuration of the exposed regions at different e-beam energy. (a): high e-beam energy penetrates the substrate, (b): low e-beam energy causes V-type writing and (c) intermediate e-beam energy produces a sharp edge writing.*

3.7 Proximity Effect

The most common problem that influences the EBL resolution is the proximity effect. The backscattered electrons could cause distortions in some of written features as well as they could produce other features in the resist itself. This case is usually called the proximity effect. As illustrated in Fig.3.4(a), due to this effect, the regions surrounding the exposed areas (black-dashed lines) are exposed again with backscattered electrons (black-solid lines), leading to slightly enlarge the exposed area.

The proximity effect was already corrected by various methods [Wue-03, Lee-05, Hu-06, Yan-09]. As this effect is related to the backscattered electrons, it can be minimized as low as possible by optimizing the e-beam energy. It can be clearly seen in Fig. 3.4(b) the backscattering effect is minimized at high energy because the electron penetrates deeply in the substrate [Bro-88].

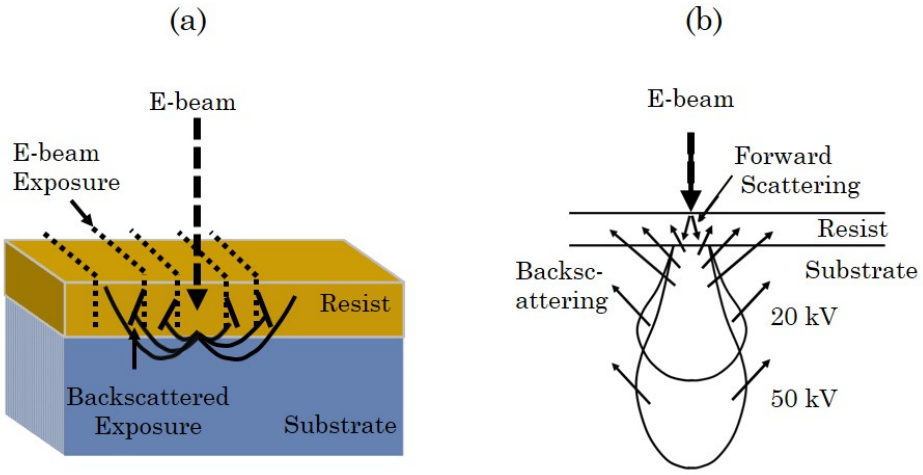

Figure 3.4: *(a) Schematic carton for the proximity effect in EBL resist. Dashed arrow is the incoming e-beam, dashed lines are the exposed lines by e-beam, the backscattered electrons designated with black-solid lines cause extra exposure as shown in the white-solid lines. (b) The interaction of an e-beam with a resist under two accelerating voltages. Backscattered electrons are reduced at higher voltage. Figure (b) is adapted with permission from [Bro-88]*

As has already been stated that when the e-beam dose increases, the feature size increases as well. Therefore, the proximity effect is increased due to the contribution of the secondary electrons emitted from the resist. Ying et al [Yin-10] have corrected a sever proximity effect occurred in a photonic crystal structure fabricated on a PMMA resist. The pattern includes holes of diameter of 200 nm and separated by 350 nm and irradiated by 10 keV e-beam. In their method all the exposure parameters (e.g. accelerating voltage) were kept unchanged while the dose was

compensated by a factor. Therefore, it is necessary to adjust the e-beam energy so that this effect can be avoided or minimized.

3.8 Development of Electron-Beam Resist

Development process allows the exposed areas to dissolve in the developer solvent. Selection of an appropriate solvent is necessary for high contrast pattern. Each e-beam resist (EBR) has an individual type of the developer. For PMMA resist, the typical high-contrast developer is 1:3 methyl isobutyl ketone:isopropanol alcohol (MIBK:IPA). The development of lines pattern is however easier than developing the hole or dot patterns because the developer is confined to penetrate through a very small exposed area of the hole. This process becomes more difficult as the diameter of the hole is a few tenths of nanometers, and hence some of the holes are not seen. In order to allow the developer to penetrate into the exposed region, the sample must be shocked during development, or using ultrasonic agitation [Arj-09].

3.9 Metallization and Lift-off Process

After development of the pattern, a metal layer is usually evaporated on the resist. Different materials are used such as gold, aluminium and etc. The pattern is then transferred to the metal after lifting-off unwanted areas of the metal. Lift-off process is shown in Fig. 3.5. A PMMA resist is spun on the substrate, and then exposed to an e-beam and developed, as shown in Fig. 3.5(a and b). A metal layer typically of a few tenth of nanometers is evaporated by thermal system or by an e-beam evaporation on the pattern (Fig. 3.5(c)).

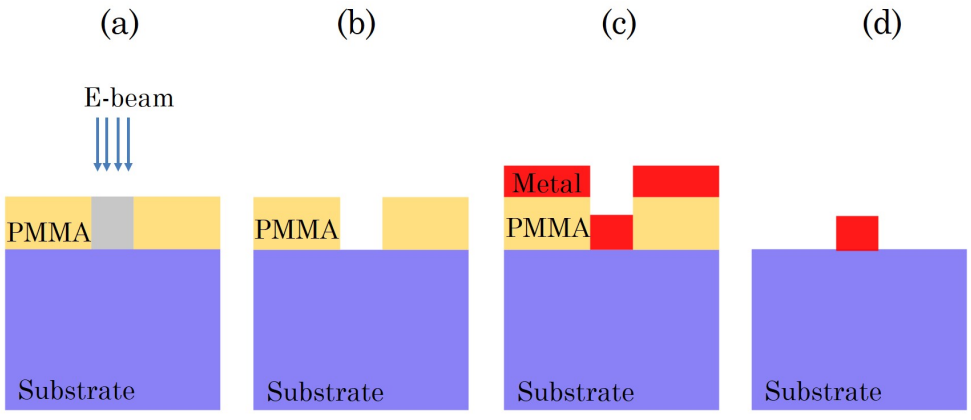

Figure 3.5: *Schematic process for transferring an e-beam resist pattern to a metal. (a) Spinning of PMMA on the substrate, (b) Development of the exposed area, (c) Evaporation of a metal layer on the PMMA, (d): Lift-off metal from the unexposed area.*

Finally, as shown in Fig. 3.5(d), by rinsing the sample in a solvent, such as acetone, unexposed resist is dissolved so that the unwanted-metal layer on it is lifted-off.

The quality of a printed pattern is fully assessed via lift-off process. That is, if the wall or bottom of the exposed area is not perfectly exposed or developed, the pattern will not be completely transferred to the metal. In a single layer process, i.e. only one layer of a resist is spun on a substrate, the lift-off is mainly dependent on the exposure dose. If the dose is low, V-type pattern in the resist can be obtained, as shown in Fig. 3.6(a). Then, the metal evaporated on the pattern will adhere to the walls of the exposed area, leading to connect the unwanted metal areas to that on the substrate, as shown in Fig. 3.6(b). In this case, the lift-off will fail to remove the unwanted metal. Another problem which makes the lift-off process difficult is using very thin resist even though it is required to produce a high resolution pattern, as previously stated. In Fig. 3.6(c), it is seen that both the upper and lower areas are attached to each other and thence the metal remains attached to the resist. Therefore, in order for a successful lift-off process, it is recommended that the resist must be thicker than the metal layer or using multiple layers of resists.

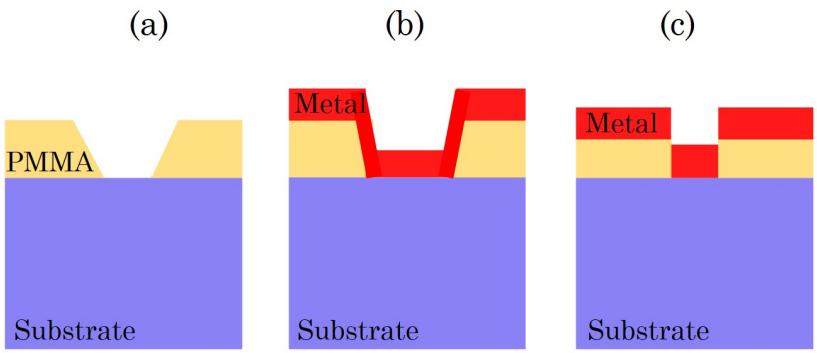

Figure 3.6: *Scheme for the lift-off metal layer. (a) V-type pattern of EBL resist, (b) Evaporation of a metal layer on a V-type resist, (c) Evaporation of a metal layer on a thin layer of resist.*

3.10 Nanowire Fabrication

Nanostructure fabrication has currently one of the most important and applicable fields of physics. Various electronic, optoelectronic and communication systems are fabricated from semiconductor nanostructures, such as nanowires, quantum dots, quantum wires and so forth. Nanowires (NWs) are one-dimensional nanostructures with high aspect ratio (the ratio of length to diameter). It may exhibit a quantum mechanical behaviour when the diameter is comparable to the electron de Broglie wavelength. NWs can be fabricated by two techniques: bottom-up and top-down.

3.10.1 Bottom-Up Method

In the bottom-up method, the growth of NWs can be achieved using a so called Vapour-Liquid-Solid (VLS) growth mechanism. This technique can be achieved either by using a metal nanoparticle as a catalyst for NWs growth or using self-catalyzed growth mechanism, in which there is no need for a metal. In metal-catalyzed VLS growth mechanism, NWs based III-V semiconductor compounds have been grown by VLS growth mechanism using different growth techniques, such as MBE [Bou-12, Alo-13], MOVPE [Moh-07, Mus-08, Zha-08, Bor-10] and chemical beam epitaxy [Zha-12].

Figure 3.7 shows a schematic illustration of the VLS growth mechanism in which metal nanoparticles are initially fabricated on a substrate. Nobel metals such as gold (Au) [Moe-08] as well as non-noble metals, such as nickel (Ni), copper (Cu) or Al [Wan-06] are mostly used for this purpose. VLS mechanism includes three material states. First, the metal nanoparticles are heated and the source material is provided as vapour of molecules or atoms. At a certain substrate temperature, the nanoparticles form alloys with the substrate and become droplets. Then, the incoming material eutectic with nanoparticles, so it transforms from vapour to liquid state. When the droplets are supersaturated with the incoming material, the latter is nucleated at the interface between the droplets and the substrate. Finally, the material liquid transforms to solid, and the growth of nanowire is initiated at liquid-solid interface. The diameter and density of NWs are controlled by the size and density of the droplets.

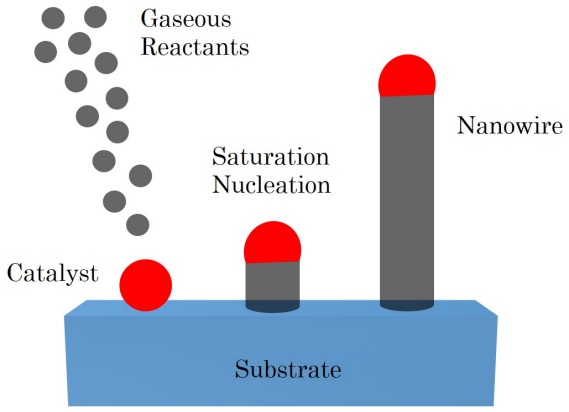

Figure 3.7: *Schematic of VLS growth mechanism of NWs. The metal nanoparticle is a liquid droplet. When the droplet is supersaturated with the incoming molecules, the material is nucleated at the interface between the droplet and the substrate to form a nanowire.*

In self-catalyzed VLS technique, one of the source materials is first evaporated on a substrate for a few seconds to form droplets as catalysts [Tat-10, Kua-12, Kro-10]. Then, at a certain growth temperature, the source materials are provided to initiate VLS growth of NWs. By this method, growth of III-V NWs was successfully achieved by different groups [Gra-13, Pli-10, Mad-11]. Also, metal problems associating growth of NWs, such as traps [Wan-06] and stacking faults [Gla-07] in NWs structure have been overcome.

3.10.2 Top-Down Method

Although VLS mechanism gives rise to high quality NWs, various defects are possibly formed during the growth process [For-10]. In addition, it is difficult to grow a limited number of nanowires that required for some applications, such as electronic-logic gates. Alternatively, top-down mechanism is another method serves such application. In this method, NWs are fabricated using a mask made of metal, photoresist or EBR on a material. Then, NWs are produced by wet-chemical etching or dry etching the material around the mask. In any type of etching, the material may isotropically, partially or anisotropically be removed. A schematic representation of the etching is shown in Fig. 3.8.

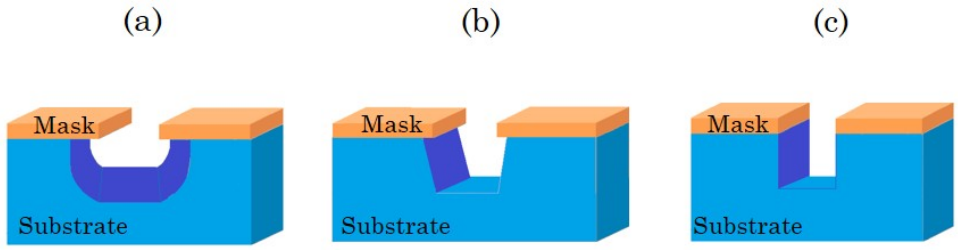

Figure 3.8: *Schematic of (a) isotropic (b) partially isotropic and (c) anisotropic etching.*

In the isotropic type, the vertical and horizontal etching are equal, while the vertical and lateral etching are different in both partial and anisotropic etching. The material removal rate in time is expressed by an etching rate (E_R), which is given as:

$$E_R = \frac{Thickness\ before\ etching - Thickness\ after\ etching}{Etching\ time}, \tag{3.2}$$

Wet-chemical etching can be performed by immersing the material in liquid chemicals or etchants. A pattern that is required for etching is defined by the mask on the material. Various types of masks can be used depending on the type of etchant. For example, photoresist of type RZJ-304 is considered an appropriate mask to protect a silicon wafer against a mixture solution of hydrofluoric acid (HF) and sliver

nitrate ($AgNO_3$) [Sun-12]. The process of wet-chemical etching involves three steps: transport of etchant to the material surface, reaction of the etchant with the surface, and diffusion of the byproducts from the surface. That is, the material is oxidized and then dissolved in the acid.

In this type of etching, the vertical etching is intersected by the slanted plane of the crystal, i.e. plane (111) in (100)-type substrate, and finally a V-shape etching will be produced (Fig. 3.8(b)). Benefiting from this feature of wet etching, a V-shaped groove was formed in Si (100) using a potassium hydroxide (KOH) solution for anisotropic etching [Yun-00]. Also, sharp-pyramidal tips were obtained by anisotropic-wet etching of Si (100) by (KOH) solution [Res-03].

The dry etching can be achieved by applying a beam of ions, electrons, or photons with high energy. By bombarding the substrate surface with high energy particles, the atoms leave the substrate. Two mechanisms of dry etching are used: physical and chemical etching. In the first type, no chemical reaction is used, while the second type a chemical reaction is allowed for achieving the etching. Figure 3.9 shows the dry etching process. The unmasked regions of the material are removed without undercut etching. In the chemical dry etching, ions of tetrafluoromethane (CH_4), chlorine gas (Cl_2), or fluorine (F_2) and etc. [Alv-05] are used.

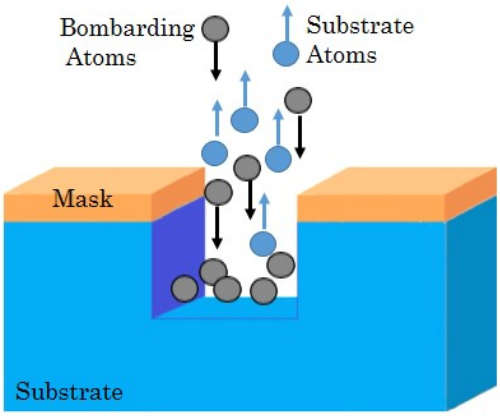

Figure 3.9: *Dry etching process in a substrate. The incoming atoms lead to remove the unmasked region of the material.*

One of the most widely used technique of dry etching is called reactive ion etching (RIE) that uses both physical and chemical mechanisms. The mechanism of the RIE etching involves reactive gases, e.g. CH_4, to produce actions, which are accelerated with high energy and then directed to the substrate. These actions chemically react with the substrate. Although dry etching is isotropic, anisotropic RIE was successfully achieved to fabricate GaP nanowires [Yan-07].

3.10.2.1 Metal-Assisted Chemical Etching

Recently, the so called metal-assisted chemical etching has gained much interest as an attractive method for the fabrication of high-aspect ratio nanostructures. In this method a noble-metal particle is used as a catalyst for MacEtch in a solution of an oxidizing agent, such as H_2O_2, and an acid such as HF. Besides the low cost of this mechanism, there is a possibility to obtain various types of nanostructures depending on the shape and size of the patterned material. It was first proposed by Li and Bohn [Li-00] as an anisotropic wet etching catalyzed by Au, platinum (Pt) or gold/palladium (Au/Pd) particles using a mixture of H_2O_2 / HF for producing porous silicon.

Thereafter, it has successfully been used to fabricate various types of nanostructure of silicon, such as Si nanowires [Bal-12, Che-10], porous Si [Cha-02, Sch-12], Si nanopillars [Wan-13]. A review of MacEtch in silicon was detailed by Huang et al. [Hua-11]. Some parameters determine the morphology of the etched structure, including the orientation of the substrate, doping, and concentration of the etching solution. It was found that p-Si (110) and n-Si (111) result in vertical nanowires. Similarly, etching of highly doped n-GaAs (100) results in high aspect nanopillars [DeJ-11]. Very recently, nanocones have been obtained by etching a GaP substrate in solution of H_2O_2 and HF [Kim-16]. NWs produced by MacEtch process is shown in Fig. 3.10.

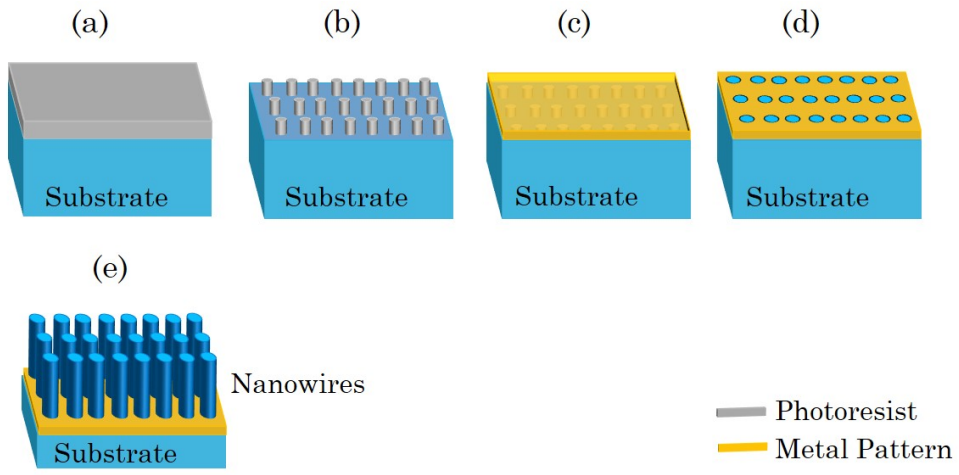

Figure 3.10: *Demonstration of nanowires fabrication by MacEtch of a substrate. (a) Spinning of photoresist on a substrate, (b) writing a pattern in the resist, (c) evaporation of metal layer on the resist, (d) lifting-off the unwanted metal, (e) etching the substrate underneath of the mask to produce NWs.*

A photoresist is spun on the substrate (Fig. 3.10(a)), printing a pattern in the resist (Fig. 3.10(b)), transferring the pattern to a thin metal layer (Fig. 3.10(c, d)),

and etching the substrate underneath the pattern to produce NWs (Fig. 3.10(e)).

Mechanism of MacEtch of Si in a mixture of H_2O_2/HF catalyzed by gold, as has already been proposed by Li and Bohn [Li-00], includes two reactions: cathode reduction at the noble-metal surface and anode oxidation at the semiconductor. Both reactions are demonstrated below: The metal catalyzes the reduction of H_2O_2 generating holes (h^+), and the reduction of (h^+) forming H_2. Subsequently, these holes are injected into the Si substrate. The cathode reaction is given by:

$$H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+, \tag{3.3a}$$

$$2H^+ + 2e^- \rightarrow H_2 \uparrow, \tag{3.3b}$$

At the anode, the injected holes oxidize the Si substrate underneath the noble-metal forming ionic products that are dissolved in HF:

$$Si + 4h^+ + 4HF \rightarrow SiF_4 + 4H^+, \tag{3.4a}$$

$$SiF_4 + 2HF \rightarrow H_2SiF_6, \tag{3.4b}$$

The overall reaction of the cathode and anode is given below:

$$Si + H_2O_2 + 6HF \rightarrow 2H_2O + H_2SiF_6 + H_2 \uparrow, \tag{3.5}$$

Dissolution of Si under the metal is dependent on the charge transfer between the injected holes and the Si substrate. This process may occur when the electrochemical potential of an oxidant is more positive than the maxima of the valence band of the substrate. Figure 3.11 [Hua-11] illustrates a comparison between the potential of the Si substrate bands and the electrochemical potentials of different oxidants. It is clear that H_2O_2 has a much more positive potential than that of the Si valence band. That is, h^+ can be injected into the Si valance band.

The above equations indicate that MacEtch of Si can arise as long as h^+ are produced disregarding the doping level of Si. The influence of doping concentration in the surface morphology of p- type Si NWs fabricated by Ag-catalyzed MacEtch has already been instigated by Hochbaum et al. [Hoc-09]. Their results showed that the rougher nanowire surface correlates to the higher doping concentration. They attributed the findings to two reasons. First, existence of crystal defects and impurities in the surface are considered nucleation sites for pore formation. With higher dopants, the thermodynamic driving force for creating pores is enhanced, and thereby the surface roughness increases. Second, as the doping concentration increases, the depletion region and the potential barrier between Ag and Si are reduced, so more charge will be transferred between them, causing an increase in the nanowire surface roughness. A successful example for Si-NWs array of 200 nm in diameter fabricated by MacEtch in a mixture of H_2O_2/HF/Ethanol and catalyzed by Au nanoparticles was presented by Balasundaram et al. [Bal-12].

In fact, regardless of silicon, MacEtch was limited to a few types of semiconductors, such as gallium nitride (GaN) catalyzed by silver (Ag) nanoparticles [Gen-12], and germanium (Ge) substrate [Kaw-13]. However, DeJarld et al. [DeJ-11] produced GaAs nanopillars of width between 500 - 1000 nm by MacEtch using Au mesh and etching solution of $KMnO_4/H_2SO_4$. MacEtch was found to be occurred beneath the Au mesh at an etching temperature between 40 - 45 °C, while no etching was seen at lower temperature.

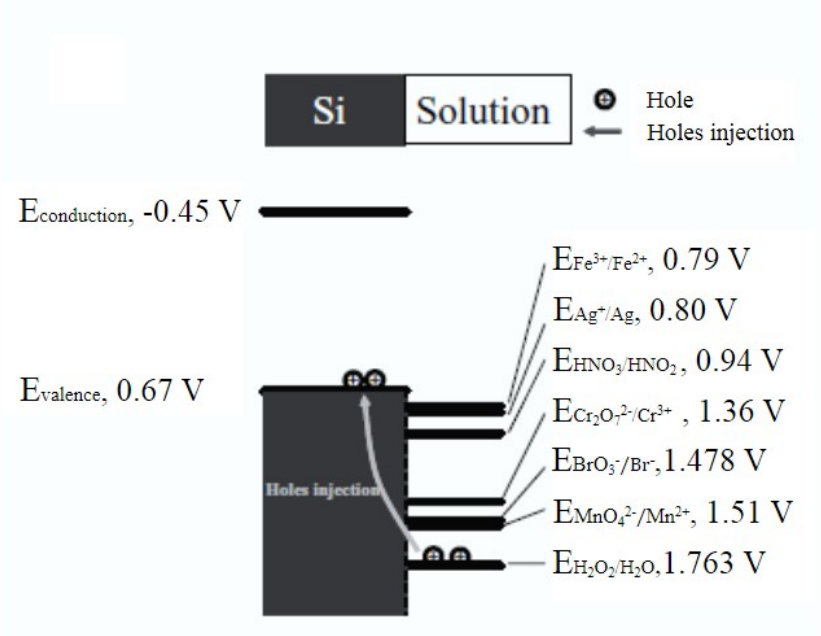

Figure 3.11: *Schematic illustration for potential of Si energy bands and the electrochemical potentials of different oxidizing agencies. The oxidant H_2O_2 has a much higher potential than that of the Si valence band. Adapted with permission from [Hua-11] (Copyright 2011, Wiley-VCH).*

CHAPTER-4

Characterization Techniques

Characterization Techniques

Introduction

Crystalline quality of a heteroepitaxial film as well as the fabrication of semiconductor devices are always evaluated via various characterization techniques. For the purpose, there exist in-situ and ex-situ characterization tools, which enable different measurements. For instance, in the MBE growth chamber, RHEED is a useful in-situ tool that can be used for monitoring the surface morphology of the layer during growth. The ex-situ tools comprise many instruments like: X-ray diffractometer, scanning-electron microscopy, atomic-force microscopy, current-voltage and capacitance-voltage setups, and noise techniques. A description of these techniques are presented in this chapter.

4.1 Reflection High-Energy Electron Diffraction

The diffraction-based analysis techniques are very significant tools utilized for understanding the crystalline properties of layers and junction interface. RHEED is the most useful tool in the MBE growth chamber utilized to monitor the surface reconstruction of the substrate during thermal cleaning, and growth progress in situ. The RHEED instrument mainly consists of an electron gun and a fluorescent screen, which detects the electrons diffracted from the surface of the sample.

As seen in Fig. 4.1, the electron is directed on the surface at a grazing angle of about $1-5^{\circ}$ relative to the parallel surface, with an energy range of $5-50$ KeV.

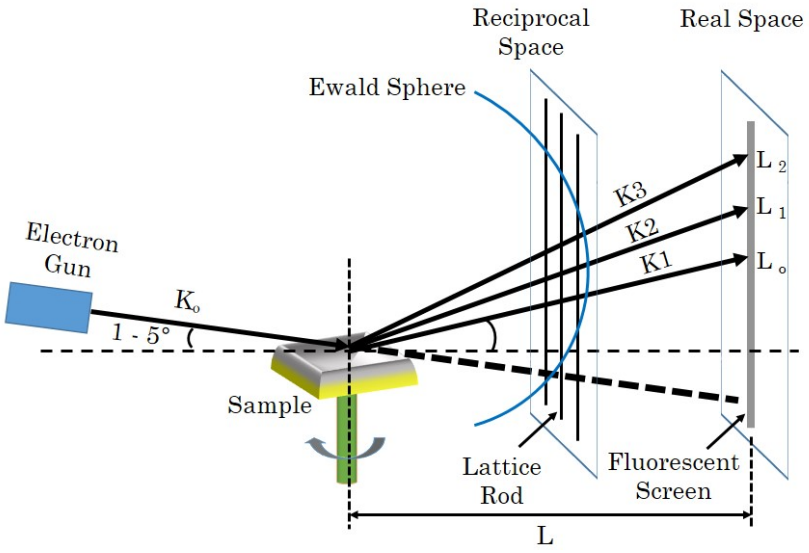

Figure 4.1: *A scheme of RHEED arrangement in MBE system. It consists of an electron gun and a fluorescent screen. A RHEED pattern can be seen by the observer on the screen.*

The de Broglie wavelength of the incoming electron is expressed by $\lambda_d = h/\sqrt{2m_eE}$, where h, m_e and E are the Plank's constant, the rest mass of electron and electron energy, respectively. Thus, for an electron of energy of 5 KeV, for example, λ_d is equal to 0.172 °A. That means the small-incident angle allows the electron beam penetrating only a few atomic layers in the surface. The incident beam is then diffracted on the screen producing a pattern demonstrating the quality of the surface. By this means, a reaction of the incident electron beam with the surface provides information about the surface morphology of the substrate or the epilayer [Yue-90, Koi-01, Ong-01], including spotty, two-dimensional (2-D) or three-dimensional (3-D) pattern. The first pattern means the surface is rough, while a smooth surface may be seen by a 2-D growth. A nonstructural layer, such as quantum dots, can show a 3-D pattern.

The diffraction of the e-beam obeys Laue condition. In Fig. 4.1, the reciprocal and real space in momentum space are shown. This arrangement is referred to as an Ewald construction, which is used to demonstrate the diffraction phenomena arise in RHEED. Consider k_0 be the wavevectors of the incident electron waves, then the diffracted wavevectors k_1, k_2 and k_n draw a sphere of radius $|k_0|$ in reciprocal lattice planes. This is referred to as an Ewald sphere. A number of circles are produced from intersection of the Ewald sphere with the reciprocal lattice planes. Thus, concentrated halves circles are seen on the fluorescent screen, while the other unseen halves circles lie in the shadow region. These circles are referred to as zero, first, and nth Laue zone (L_0, L_1... Ln). Finally, small spots are seen on the screen, which reflect the lattices of surface reconstruction.

4.2 X-Ray Diffraction

In 1895, the German physicist Wilhelm Röntgen discovered X-ray, and then developed for medical, scientific and civil purposes. For physical and chemical applications, the X-ray diffraction was discovered by Max von Laue in 1912, and used to study crystal properties of materials. Information regarding bulk properties like lattice constant of crystal, strain and relaxation of a layer, grain size, defects density and etc. can be obtained by diffraction curves. In synchronous with the Laue discovery, the diffraction condition was mathematically formulated in so called Bragg law.

4.2.1 Bragg's Law

The X-ray diffraction (XRD) measurements are performed by an XRD diffractometer using the monochromatic CuKα line of 1.54056 °A. When an X-ray beam is incident on a sample, X-rays with the same wavelength as the incident are scattered, in addition to arising other phenomena like absorption. Such type of scattering is

called coherent scattering. The structure of a material is determined by the intensity and distribution of the XRD peaks.

When an X-ray beam of wavevector (k_I) strikes a crystal plane with an incident angle (θ), the diffraction condition is satisfied provided that the diffracted ray ($k_\circ$) makes the same angle as the incident ray. This case is shown in Fig. 4.2(a).

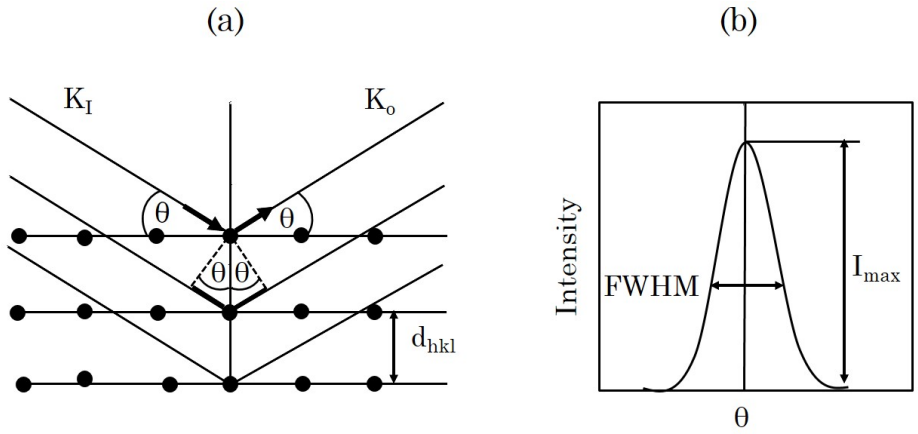

Figure 4.2: *(a) Diffraction of X-rays by crystal planes. (b) Diffraction peak of X-rays at Bragg's angle θ. d_{hkl} is the distance between two crystal planes for Miller indices h, k and l.*

Thereby, according to Bragg's law:

$$n\lambda = 2d_{hkl}\ sin\theta_s, \tag{4.1}$$

where λ is the wavelength, n is a number referred to the order of reflection plane and d_{hkl} is the distance between two crystal planes, which is related to lattice constant (a) by:

$$d = \frac{a}{\sqrt{h^2 + k^2 + l^2}}, \tag{4.2}$$

where (hkl) are the Miller indices of the diffraction plane. For a single wavelength, the first-order reflection (n=1) is typically expressed in XRD pattern. When the diffraction condition is satisfied, constructive interference results. Consequently, the diffraction peak of a high quality crystal shows a delta function of intensity (I), as shown in Fig. 4.2(b). Practically, a broad peak is seen due to crystal defects, such as high-density dislocations in the layer, or instrumental imperfections like high divergence the X-ray beam. The full-width at half-maximum (FWHM) of the peak is typically considered one way to evaluate the quality of the material. For example, the narrower FWHM is the highest quality layer.

4.2.2 X-Ray Geometry

There are two types of X-ray scans used for obtaining information about crystal structure: symmetric and asymmetric scans. The first one provides information about perpendicular lattice parameter, while the asymmetric geometry enables one to measure the parallel lattice parameters. One of the well-known XRD geometry is called a double-axis diffraction, and shown in Fig. 4.3(a).

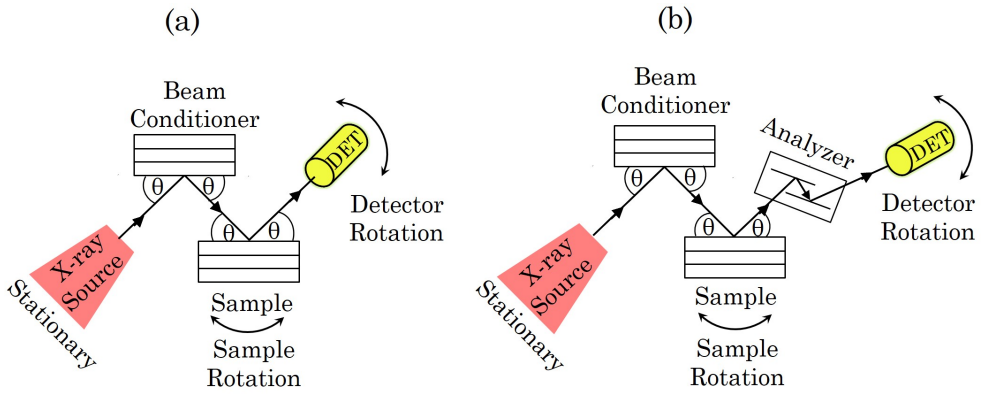

Figure 4.3: *Configuration of XRD measurements. (a) Double-axis diffraction and (b) triple-axis diffraction, in which the analyzer in used to get one high resolution peek at Bragg's angle θ. DET: detector.*

This arrangement consists of two successive axes: one is a beam conditioner, which is a reference crystal of a certain diffraction plane, e.g. (hkl:100), and the second is the sample crystal. The X-ray is incident on the reference crystal, and then it is diffracted with the same incident angle (θ). The diffraction condition is satisfied when the sample is rotated so that its diffraction plane becomes in parallel to the reference plane.

Another type of the geometry is called a triple-axis diffraction. It is similar to the previous arrangement, except it has an analyzer in front of the detector, as shown in Fig. 4.3(b). The difference between the double-axis and triple-axis geometry is related to the user. That means, to figure out different Bragg peaks for multilayers, double-axis geometry is preferred. While, for a higher resolution one Bragg peak, the second geometry is required because the analyzer will restrict the X-rays to reach the detector except at a certain Bragg's angle.

4.2.3 Symmetric XRD

This type of XRD geometry includes $\theta/2\theta$ and ω-scans. Both scan types are described below.

4.2.3.1 $\theta/2\theta$ Scan

The schematic arrangement of $\theta/2\theta$ scan is illustrated in Fig. 4.4(a). The wave vector of the incident ray, the diffracted ray and the scattering ray are referred to as K_I, $K_\circ$ and K, respectively. In this arrangement, the X-ray source is stationary while the sample rotates with an angle θ and the detector rotates in synchronous with the sample rotation with an angle 2θ with respect to the extension of K_I (dashed arrow).

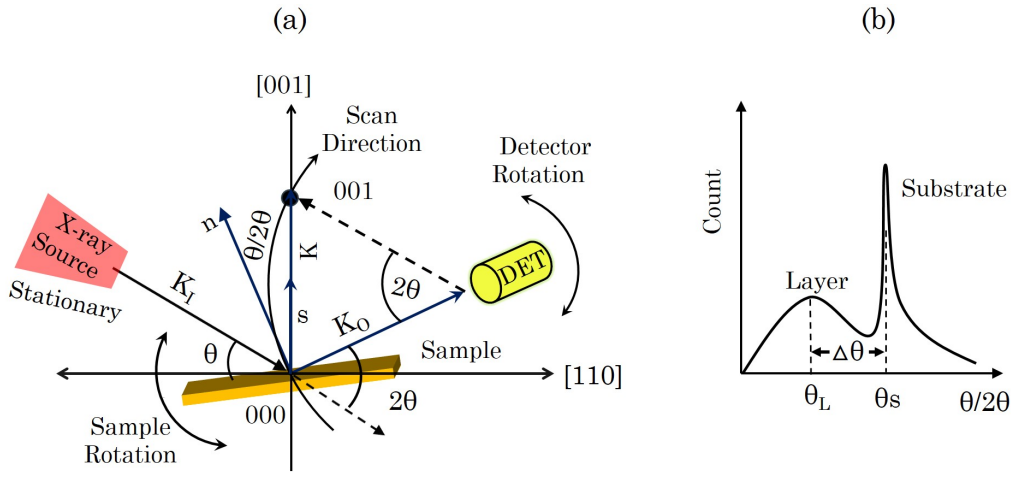

Figure 4.4: *Schematic arrangement for $\theta/2\theta$ scan (a). K_I is the incident wave vector, $K_\circ$ is the diffracted wave vector, K is the scattering wave vector, n is a normal surface vector, and θ is the incident angle. (b) $\theta/2\theta$ XRDs for two materials. $\Delta\theta$ is the peak splitting between the layer and substrate.*

In this type of scan the magnitude of K ($|K| = |K_\circ - K_I|$) varies depending on the value of θ, while its direction is always parallel to the surface normal (S) in the Ewald sphere. Thus, the intensity of the rocking curve changes as the value of θ changes. By performing this scan, more than one XRD Bragg peaks may present depending on the number of the materials. It is also called ω/θ scan, where $\omega = \theta$. From a $\theta/2\theta$ scan for two materials, e.g. layer and substrate, shown in Fig. 4.4(b), $m_\perp$ can be calculated from their peak splitting ($\Delta\theta$) as:

$$m_\perp = -\Delta\theta \; cot\theta_B. \tag{4.3}$$

4.2.3.2 ω-Scan

It is sometimes called a rocking curve scan. This type of XRD scans is usually performed to record one strong Bragg angle peak of a certain diffraction plane of a crystal under test. A schematic arrangement of ω-scan is illustrated in Fig. 4.5. The detector is fixed at the expected Bragg angle position (θ), and the scan is performed

by rocking the sample with an angle (ω). The magnitude of scattering wave vector K is constant while its direction varies along the arc shown in the figure (scan direction) depending on the value of ω. When the surface makes the exact Bragg angle, the diffraction peak can be seen.

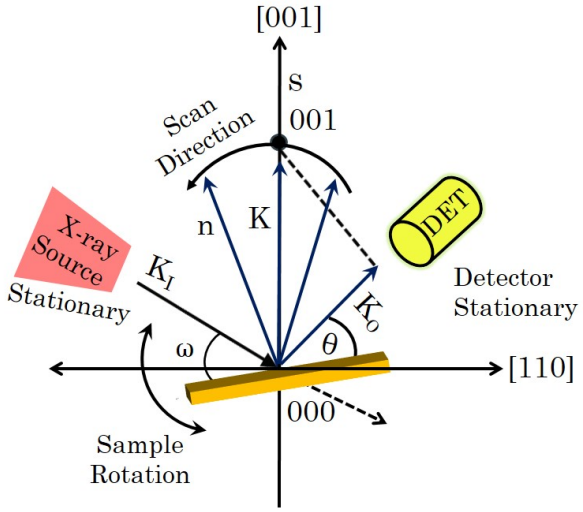

Figure 4.5: *Schematic arrangement for ω scan. K_I is the incident wave vector, $K_\circ$ is the diffracted wave vector, K is the scattering wave vector, and θ is the angle between the incident beam and the sample surface.*

4.2.4 Asymmetric XRD

The asymmetric XRD geometry comprises grazing incidence (GIXRD) and grazing exit (GEXRD) $\omega/2\theta$ scans. These scans are used for the determination of structural properties of semiconductor films and nanostructures including in-plane lattice parameters, grain size, tilt in the layer, etc. According to Beer-Lambert law, when an X-ray beam of intensity $I_\circ$ strikes a surface perpendicularly, the transmitted intensity decreases exponentially from the surface by:

$$I = I_\circ \, e^{-\mu x}, \tag{4.4}$$

where μ and x are the material linear-attenuation coefficient and penetration depth in the material. If the beam is attenuated in the material to about 37% (1/e) of the incident value, the depth of the penetration is inversely proportional to the attenuation coefficient, i.e. $(x = 1/\mu)$. When the beam hits the surface at an arbitrary small angle, say ω, the penetration depth is reduced to $x = sin(\omega)/\mu$ [Alt-12]. The X-ray beam will penetrate only a few nanometers. That is, the beam can interact in the atomic layers that close to the surface, and thereby information about the surface morphology are obtained from the measurement.

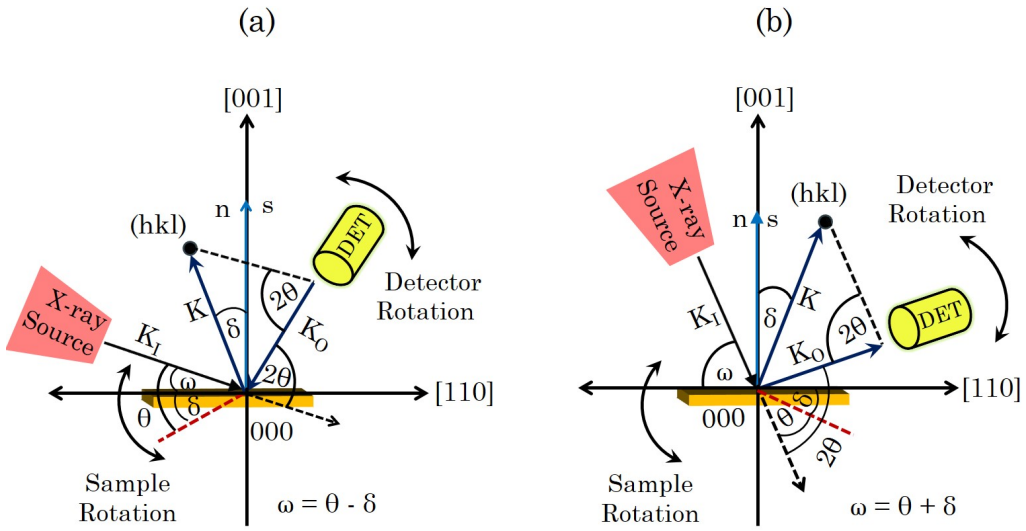

Figure 4.6: *Reciprocal space configuration of $\omega/2\theta$ XRD scans for grazing incidence (a) and grazing exit (b). K_I is the incident wave vector, $K_\circ$ is the diffracted wave vector, ω is the angle between the incident beam and the surface and δ is the inclined angle of the reflection plane ($\delta = \theta - \omega$).*

A configuration for the GIXRD measurement is shown in Fig. 4.6(a). The incident angle (ω) between the wavevector K_I and the sample surface is small, while the diffracted ray $K_\circ$ makes a large angle with the surface of the sample. The scattering angle 2θ is surrounded between $K_\circ$ and the extension of the incident ray (dashed arrow). During scanning, the angle (ω) is kept constant while the angle θ is changed and the detector is moved around 2θ.

The GEXRD measurement configuration, shown in Fig. 4.6(b), look likes a GIXRD arrangement rotated by an angle of 180 ° around the surface normal. The incident angle ω is thus large, while a small angle is made between $K_\circ$ and the surface of the sample. The scanning process is performed by rotating the sample and detector synchronously. These scans are called radial scan because the direction of vector K with respect to the surface normal remains fixed during the whole measurements. The in-plane parameters of the layer can be calculated from an asymmetric $\omega/2\theta$ XRD measurement in a reflection plane makes inclination angle δ_S with the surface plane of the substrate (we consider $\delta_S = \delta$). When the layer crystal has an orthogonal shape, $a_\perp$ and $a_\parallel$ can be calculated from asymmetric XRD [Slu-93] as:

$$a_\perp = a_S \frac{\cos\delta_S \ \sin\theta_S}{\cos\delta_L \ \sin\theta_L}, \tag{4.5}$$

$$a_\parallel = a_S \frac{\sin\delta_S \ \sin\theta_S}{\sin\delta_L \ \sin\theta_L}. \tag{4.6}$$

The angle δ_L is the inclination angle of the layer; the angle surrounded between the

surface plane and the reflection plane of the layer. For diffraction planes in the same family such as (115) and (-115), the angles θ_L and δ_L are given as [Twe-10]:

$$\theta_L = \theta_S - \frac{\Delta\omega_i + \Delta\omega_e}{2}, \tag{4.7}$$

$$\delta_L = \phi_S - \frac{\Delta\omega_e - \Delta\omega_i}{2}, \tag{4.8}$$

where $\Delta\omega_i$ and $\Delta\omega_e$ are the angular splitting between the substrate and the layer peaks in grazing incidence and grazing exit, respectively. ϕ_S is the inclination angle of the substrate reflection plane.

4.2.5 Reciprocal-Space Map (RSM)

An interesting method for the characterization of an epitaxial layer is the use of so called reciprocal-space mapping (RSM). Significant information comprising crystal structure, relaxation degree, and strain status can be provided by RSM. In this map, the $\omega/2\theta$ radial scan can be visualized in the plane of momentum transfer by the two Cartesian coordinates: in-plane (Q_x) and out-of-plane (Q_z) coordinate, as shown in Fig. 4.7.

Practically, the diffraction intensity is collected from successive asymmetric $\omega/2\theta$ scans by increasing ω and θ by $d\omega$ and $2d\theta$.

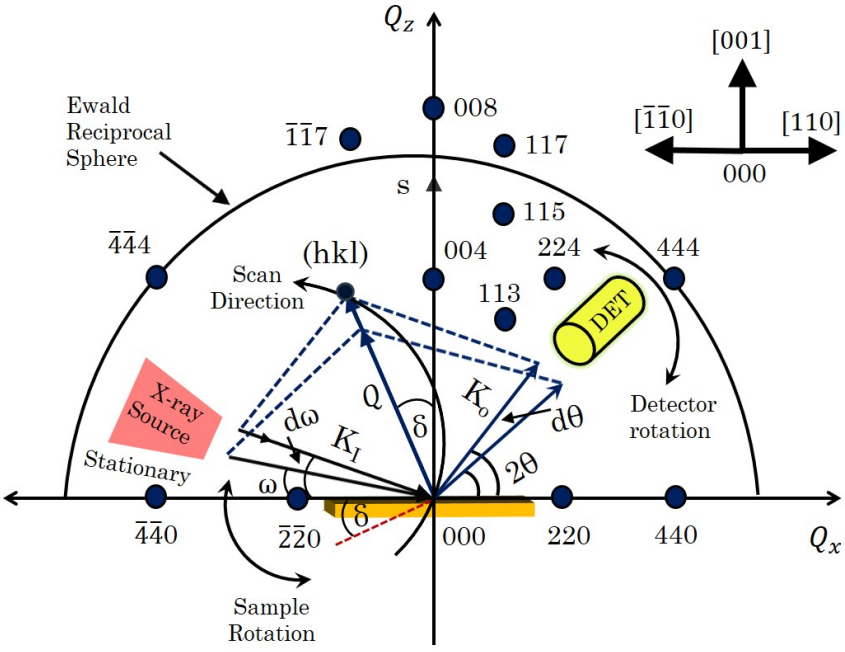

Figure 4.7: *Two-dimensional radial-scan representation for $\omega/2\theta$ grazing incidence XRD. Q_x and Q_z are Cartesian coordinates and Q is the scattering wave vector, which has a fixed direction respect to the surface normal.*

The values of the instrumental coordinates (ω and θ) during measurements are converted to the map coordinates by using the equations:

$$Q_z = 2k(sin\theta\ cos\delta), \tag{4.9}$$

$$Q_x = 2k(sin\theta\ sin\delta), \tag{4.10}$$

where $k = 2\pi/\lambda$ is the wave vector and λ is the wavelength of the X-ray, and $(\delta = \theta - \omega)$ is the angle of the diffraction plane relative to the surface plane of the crystal under test, which is in parallel to reference crystal plane. The scattering vector is the sum product of the coordinate vectors, $|Q| = |Q_x + Q_z|$.

The data collected from the scanning process, that consists of Q_x, Q_z and the intensity, are then plotted in the map. The resulted map is fully recognized by representing the scattering vector in Ewald reciprocal space. Figure 4.7 also shows the Ewald reciprocal space for a silicon wafer of orientation (001). The coordinates Q_x and Q_z are oriented in the directions [110] and [001], respectively.

4.3 Scanning-Electron Microscope (SEM)

This system is one of the most versatile instruments used for imaging the objects, surface morphology and interfaces between the layers down to nanometer scale. Also, it is a significant equipment used for the e-beam lithography. Figure 4.8 is a photograph for JOEL JSM 6360 SEM that was used for our measurements.

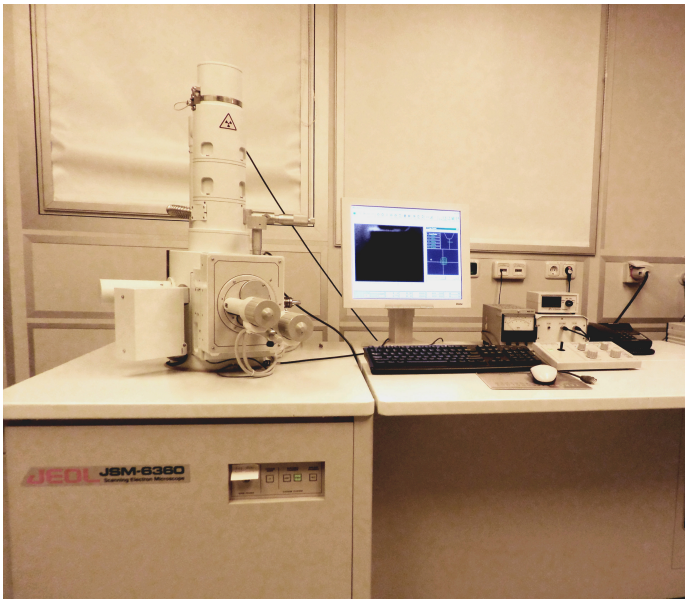

Figure 4.8: *Photograph for the JOEL JSM 6360 scanning-electron microscope that was used for the experiments of this thesis (FET group/Humboldt-University in Berlin).*

The SEM system usually operates in vacuum between 10^{-4} and 10^{-6} Torr. As has already been demonstrated in Sec.3.3, the electron gun is composed of a tungsten wire filament surrounded by a cylindrical grid to control the number of emitted electrons and an anode plate to accelerate the electrons to the sample. In the SEM systems, there exist several electromagnetic lenses to reduce the beam-spot size. These lenses are called condenser. When the beam passes through the condenser lenses, it is moved in the X and Y-directions by two magnetic scanning coils. A small aperture of a few of microns in diameter is used to minimize the electron beam diameter. Another magnetic lenses are also used to correct the astigmatism of the e-beam. Adjusting the magnification of the SEM is dependent on the dimensions of the area to be scanned. If the area is small, the magnification is increased. A certain magnification may be performed by adjusting the distance between the sample and the objective lens.

When an e-beam hits a sample under test in the vacuum chamber, the beam causes different kinds of emissions. Figure 4.9 shows the interaction of e-beam with a material. Backscattered, secondary and Auger electrons, photons, and X-rays are emitted as a result of such interaction. The backscattered electrons are re-emergent form a material when the electrons of the beam collide with material atoms. These electrons have high energies and they are functions of the material atomic numbers. The secondary electrons are low-energy electrons produced by the ionization of material atoms, especially near the surface. These electrons are detected so that the image is usually utilized for studying the surface morphology or the interface.

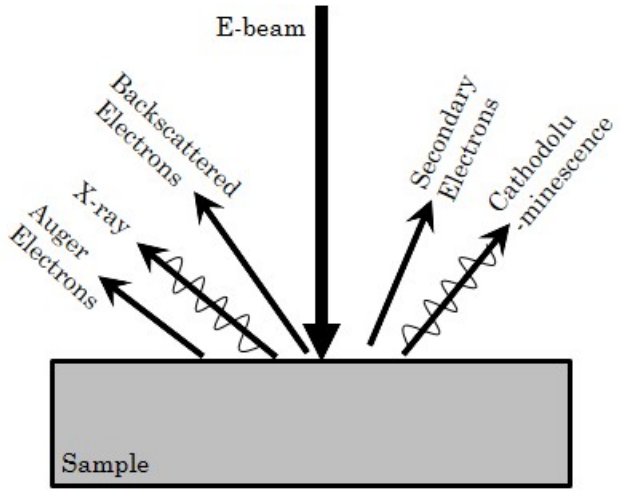

Figure 4.9: *Interaction of an e-beam with the material in the SEM chamber. Secondary electrons, backscattered electrons, Auger electrons, photons and X-ray are generated due to reaction of e-beam with the atoms of the sample.*

4.4 Atomic-Force Microscope (AFM)

AFM system consists mainly of a cantilever, laser, position-sensitive photodiode detector (PSPD) and a data processor. The surface is scanned in AFM by a tip of a diameter less than 10 nm located at the free end of a cantilever of a about 200 μm in length. During scanning, the cantilever can be precisely deflected a distance (d) depending on the surface morphology. The deflection distance is measured by a laser spot reflected on the PSPD. Between the tip and the surface, a force F is formed, which can be described by Hooke's law:

$$F = -k_s d, \tag{4.11}$$

where k_s is the cantilever spring constant. Figure 4.10 illustrates a scanning process of AFM and operational modes of AFM depending on the distance between the tip and the surface. AFM operates in three types of the operational modes. The first one is called a contact mode, in which the tip touches the surface. The second type is a non-contact mode, where the tip vibrates close to the surface. The last mode is referred to as a tapping mode when the tip is away from the surface. The scanning starts when the tip gently touches the surface and records the force between them. If the tip is far from the surface (the third mode), an electrostatic attractive force is formed between them, and the laser spot lies at long distance (d). Then, the tip approaches the surface (the second mode) and when it becomes close enough to the surface, the laser spot goes down at position (a).

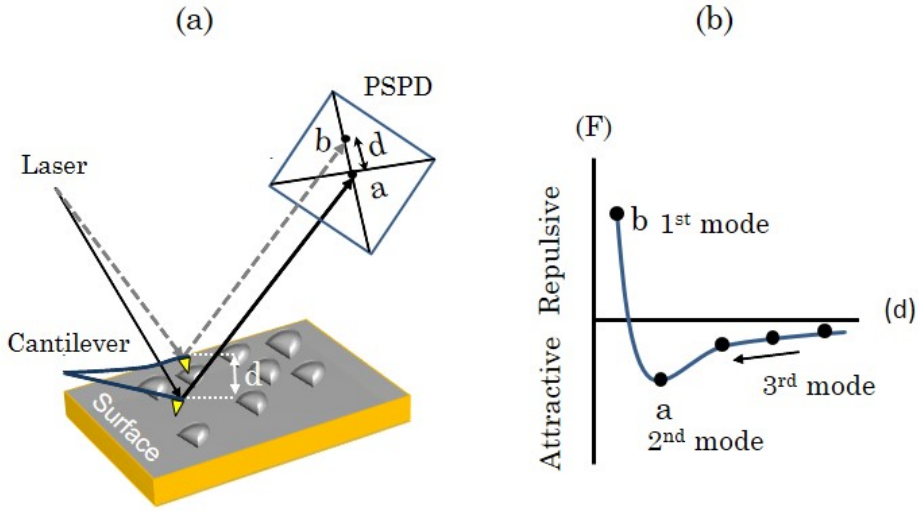

Figure 4.10: *(a) A schematic representation of AFM scanning process and (b) operational modes of AFM. Three operation modes are described for scanning the surface when the tip gently touches the surface. With scanning the sample, the laser signals are processed to plot the surface morphology.*

When the tip touches the surface (the first mode), a repulsive force is applied and thence the laser spot lies at position (b). With scanning the sample, the laser signals are processed to correlate the surface morphology.

4.5 Electric Measurements

Various electrical measurements are usually made to determine the transport properties of semiconductor films. These almost include current-voltage $(I-V)$ and capacitance-voltage $(C-V)$ measurements. In both of them, the current and capacitance is measured versus an applied voltage. Significant physical parameters can be calculated from such measurements, such as the charge carrier concentration.

4.5.1 Current-Voltage Characterization

Figure 4.11(a) shows the apparatus and the electronic circuit for $(I-V)$ measurements using a source-measure unit (SMU). This unit usually offers an ability for the $I-V$ characterization at low current (sub picoamperes). A Keithley-236 multimeter is used for the measurements, which enables a long range of voltage, e.g. 110 V. This type of SMU consists of three instruments: voltage source, current source and sensitive current and voltage meters. As illustrated in Fig. 4.11(b), the voltage is applied to the device under test (DUT) between the terminals Output HI and Output LO of SMU. The $I-V$ curve can be plotted on a computer or exported as ASCII file.

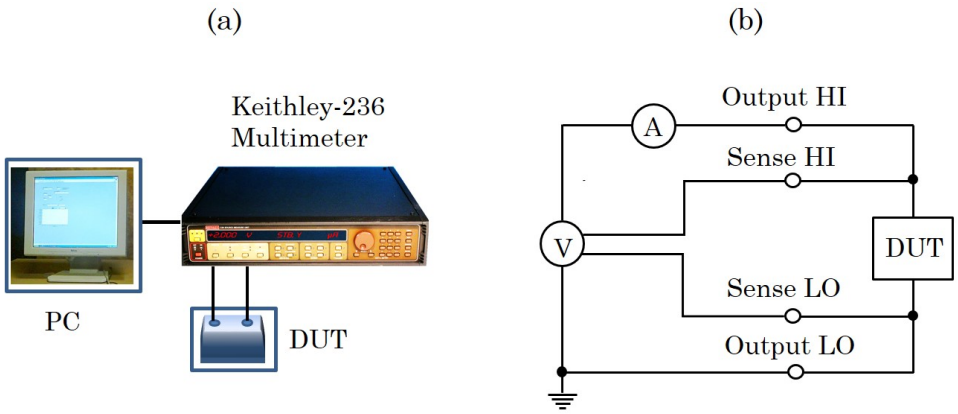

Figure 4.11: *(a) The apparatus and (b) block diagram of electronic circuit for $I-V$ measurement. DUT: device under test, A: ammeter, V: voltmeter, Output HI / LO: positive/negative terminals, Sense HI / LO: sensing remote.*

4.5.2 Capacitance-Voltage Characterization

With the presence of different semiconductor devices, it was necessary to estimate the carrier concentration and doping profile of the devices. One method is the use of $(C-V)$ measurements to estimate the majority carrier concentration in semiconductors accurately, as well as to obtain the majority carrier distribution as a function of the depth in a semiconductor. This method is applied to $p-n$ junction [Ott-10], Schottky diode [She-02, Ali-13, Red-13], quantum dots [Chi-02], metal-oxide-semiconductor field effect transistors (MOSFET) [Jan-05], solar cells [Rec-06] and graphite oxide thin films [Lee-09] and heterojunction bipolar transistor [Mit-05].

The setup of $C-V$ measurement is shown in Fig. 4.12. The sample terminals are connected to the input of a HP-4192 LCR meter, which is computerized using a LabVIEW-8.2 software. Low-temperature $C-V$ measurements can be carried out by mounting the sample holder on a metallic stage that is cooled down by a liquid nitrogen. The temperature is measured by a temperature sensor of type Pt-100 fixed on the sample stage and connected thermometer of type GMH 3710.

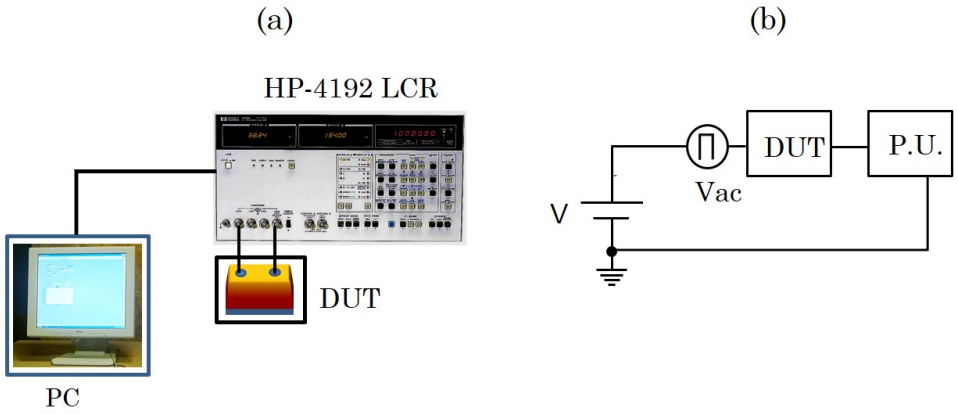

Figure 4.12: *(a) The apparatus and (b) block diagram of electronic circuit used for $C-V$ measurement. DUT: device under test and P.U: processing unit.*

The capacitance measurement is possible to sub femtofarads. A LCR meter measures the current passing through DUT and the voltage across it. Basically, the capacitance of a device is the change in the charge of DUT to the voltage (V) across its terminal. Therefore, by applying an alternative voltage signal (AC) (few tens of millivolts) to DUT, the capacitance is calculated by integrating the current flowing through the device to the voltage. That is;

$$c = \frac{dq}{dv} = \int i \frac{dt}{dv} \tag{4.12}$$

Accordingly, $C-V$ measurements for the semiconductor devices can be performed using an Ac voltage signal superimposed on a direct voltage (DC). This technique allows measuring the capacitance at different depths in the semiconductor.

4.6 Low-Frequency Noise Measurements Setup

Low-frequency noise measurements were carried out using TeachSpin's noise fundamental setup, shown in Fig. 4.13(a). The setup consists of low-level electronics (LLE) unit, high-level electronics (HLE) unit and temperature panels. The latter is composed of a metallic cavity, copper probe immersed in a liquid nitrogen Dewar, and a 50 Ω heater. In the cavity, DUT is well isolated from disturbances of electrical measurement equipment. It's temperature can be adjusted in the range of $80 - 373$ K, and measured by GMH 3710 high-precision digital thermometer. The noise current generated in DUT is fed to a current-voltage preamplifier circuit in the LLE unit. The preamplifier was modified for a vertical arrangement structure, where the GaP layer is upward and Si substrate is downward. Such arrangement enables us to characterize the GaP/Si heterostructure interface thanks to the epilayer. In the HLE unit, the noise voltage is filtered within the frequency range of 10 Hz and 100 kHz, and then amplified in the HLE unit and monitored on GS 1172 digital oscilloscope, as shown in Fig. 4.13(b). The time-domain voltage data taken from the oscilloscope are converted into frequency-domain data and analyzed using fast Fourier transform (FFT).

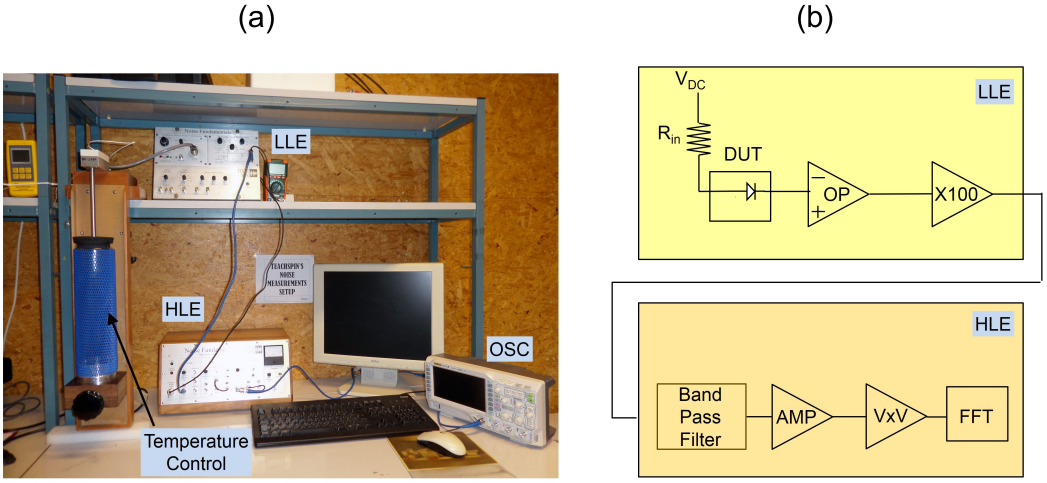

Figure 4.13: *(a) The set-up of the TeachSpin's noise fundamentals and (b) block diagram of the electronic circuit used for the noise measurements. DUT: device under test, Op: operational amplifier, AMP: amplifier and FFT: fast Fourier tranform.*

CHAPTER-5

Heteroepitaxial Growth of GaP on Si Substrate

Heteroepitaxial Growth of GaP on Si Substrate

Introduction

It has already been mentioned that the growth of GaP on Si could produce various crystalline defects. If the defects create in the heterostructure film, undesirable performance related to the optical and transport properties of the film will necessarily be obtained. The interface dislocations, for example, are common defects that play a crucial role in the conductivity of semiconductor devices. Hence, many works were already achieved to improve the quality of GaP/Si [Lee-97, Nar-02, Dix-08, Yam-09, Jus-12, Lin-13], but nevertheless this issue is still under investigation. However, the quality of the film is considerably related to various growth parameters. The most significant parameters, including growth temperature, layer thickness and thermal annealing are usually discussed. When a GaP layer is grown on a Si substrate, the layer may either be strained or relaxed relative to the substrate. If a strain relaxation arises in the layer, the dislocations would be induced at the interface between the layer and the substrate, and in the layer itself. Therefore, different cases are studied: strain, partial relaxation and fully relaxation. This chapter describes the growth mechanism of GaP/Si films at different growth conditions. The dependence of the crystal quality of the films on the layer thickness and thermal annealing is intensively studied.

5.1 Experiments

Epitaxial growth of GaP layers on silicon substrates was performed using a RIBER-32P GSMBE system. The wafers, from Virginia Semiconductor Inc., are p-type Si of orientation (100) with a miscut of 4° toward [011] direction. The substrate misorientation is useful for suppression of anti-phase domain defects [Sog-93]. Two material sources were used: solid gallium and phosphine gas. The gallium can be evaporated in the effusion cell at a temperature of 935 °C, whereas the phosphine gas is cracked at 850 °C to provide phosphorous (P). The experiments are described below.

5.1.1 Cleaning of Silicon Wafers

To promote a heteroepitaxial growth of GaP/Si, the surface of silicon wafer must be cleaned from contaminants and impurities due to wafer fabrication. Contaminated materials, such as carbon, can influence the surface morphology and form defects in the films during growth process. Moreover, the Si wafer is always covered by a native oxide layer that must be removed. Anyhow, some of the contaminants can be eliminated by chemical solvents, whereas some of them, e.g. carbon atoms, require high-temperature thermal annealing. Therefore, to ensure preparation of a clean surface, chemically and thermally cleaning the wafer have to be executed be-

fore initiating growth. The wafers were chemically cleaned by modified RCA (Radio Corporation of America) [Yu-04] using sulfuric acid H_2SO_4 (96%), hydrogen peroxide H_2O_2 (36%), hydrochloric acid HCl (32%), and hydrogen fluoride HF (50%). The procedure was carried out as follows.

1. The wafer was firstly put in a Pyrex beaker of acetone in an ultrasonic cleaner (US), at room temperature for 10 min. This followed by rinsing the wafer in deionized water (DI). This process allows removing the dust from the wafer surface.

2. Then, the wafer was dipped in a mixture of H_2SO_4:H_2O_2 (4:1) ml, placed in US at 50 °C for 10 min. The reaction was terminated by washing the wafer with DI water. This process is recommended for cleaning the Si wafer from organic contaminants.

3. Thereafter, the wafer was immersed in a hot mixture of HCl:H_2O_2:H_2O (1:1:5) ml placed in US for 10 min, and followed by cleaning with DI water. This process can help to remove ionic and metallic contaminants from the wafer surface.

4. For removing the native oxide layer from the wafer surface, the wafer was submerged in a mixture of HF:H_2O (1:20) ml contained in a Teflon beaker and placed in US, at room temperature for 60 sec, followed by rinsing it in DI water. However, this step is not sufficient to completely remove the oxide from the surface.

5. Finally, the wafer was dried by N_2 gas.

Soon after finishing the chemical cleaning, the Si wafer was loaded to the load-lock chamber and baked at a temperature about 200 °C for one hour. This process allows evaporating the water molecules attached to the surface due to chemical cleaning process. Then, it was transferred to the growth chamber with a pressure of about 3×10^{-8} Torr. In situ thermally cleaning the substrate was carried out at a temperature of 930 °C for 30 min. During this period, it was observed that the RHEED pattern of the Si surface changed gradually to a (2x1) reconstruction, confirming desorption of the residual native oxide [Yu-04, Gos-03].

5.1.2 Epitaxial Growth of GaP on Si Substrate

After thermally cleaning the substrate, its temperature was lowered to the growth temperature between 250 and 550 °C. The growth was initiated at a given T_g by introducing PH_3 with a flow rate of 4 sccm for 3 min to form a P-prelayer on the substrate, and followed by opening the Ga shutter. The prelayer enables self-annihilation of APDs [Twe-10] and it is expected to form nucleus centers for the

GaP growth [Dix-06]. Once Ga was introduced, a spotty RHEED pattern of GaP islands was observed on the substrate. The growth rate for all the samples was kept at about 0.96 μm/h.

Some samples were in situ thermally treated. Two methods of thermal annealing were compared: annealing at a constant temperature and step-graded annealing (SGA). The first method is familiar, where the grown film was annealed at a temperature higher than T_g for a time. The second method has been recently proposed in this thesis [Hus-15], in which the temperature was increased gradually for 60 and 90 min.

The structural properties of the films were characterized using symmetric and asymmetric XRD measurements performed by Bede QC1a and Philips X-Pert MRD diffractometers of sources of CuKα1 (1.5406 °A). The first one was set for 004 reflection with a GaAs beam-conditioning reference crystal, and the second was equipped with a beam monochromator for asymmetric 224, 115, 044 reflection planes. Also, the surface morphology of the GaP epilayer and the interface of the GaP/Si films were imaged using JEOL JSM-6360 and Hitachi S4800 SEM systems, and NT-MDT AFM system. The transport properties of the heterostructures were characterized using electrical and noise measurements utilizing the setups described in Sec. 4.5 and Sec. 4.6.

5.2 Effect of Growth Temperature

The growth temperature effect on the structural properties of the epilayers was investigated via growth of GaP/Si films at temperatures of 550, 400 and 250 °C. Their growth conditions and the out-of plane lattice parameters $\varepsilon_\perp$, $a_\perp$ and $m_\perp$, calculated using Eq. 4.3, Eq. 2.4 and Eq. 2.5, are listed in Table 5.1.

Sample No.	T_g $^\circ C$	h nm	$m_\perp$ %	$a_\perp$ $^\circ A$	$\varepsilon_\perp$ 10^{-3}
S1:1846	550	538	0.187±0.0003	5.4411 ±0.00005	-1.779 ± 0.009
S2:1848	400	544	0.234 ±0.0007	5.4437 ±0.0001	-1.302 ± 0.018
S3:1849	250	552	0.505 ±0.0001	5.4585 ±0.0006	1.410 ± 0.11

Table 5.1: *Growth conditions of the GaP/Si heterostructure samples S1:1846, S2:1848 and S3:1849. T_g is the growth temperature, h is the epilayer thickness, $m_\perp$ is the perpendicular lattice mismatch, $a_\perp$ is the perpendicular lattice parameter of the layer and $\varepsilon_\perp$ is the perpendicular strain of the layer.*

In Fig. 5.1, the $\theta/2\theta$ scans of the reflection plane (004) for the GaP/Si films grown

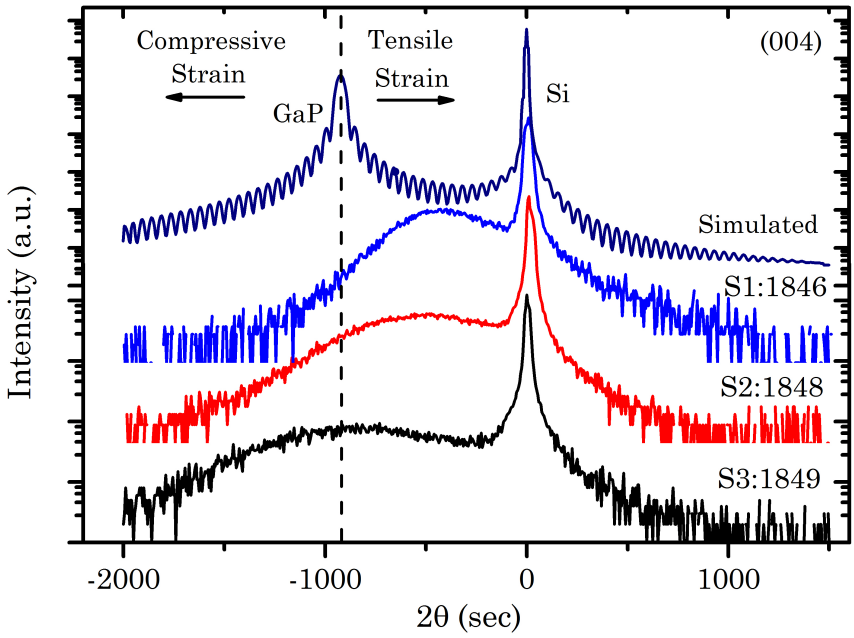

Figure 5.1: *The XRD curves of the reflection plane (004) of the GaP/Si samples grown at 550 °C (S1:1846), 400 °C (S2:1848) and 250 °C (S3:1849) as well as a simulated curve for GaP/Si using a GaAs (004) beam-conditioner.*

at these temperatures as well as the simulated curve using a GaAs (004) beam-conditioner are demonstrated.

It is seen that the full-width at half-maximum of the epilayer peak decreases with the increase of the growth temperature. At T_g = 250 °C (sample S3:1849), the peak is highly broadened with a lower intensity in comparison to the other peaks. Alternatively, when the temperature increases, the peak position of GaP approaches the Si peak. Therefore, according to the diffraction Bragg's law, the closest peak seen at the highest growth temperature gives rise to decrease the perpendicular lattice parameter. That is, the epilayer could be contracted perpendicularly and expanded horizontally.

In the simulated curve, the GaP peak matches the peak position of the bulk GaP crystal (dashed line). Let us compare this peak with the experimental peaks. Two cases could possibly happen. First, if the layer peak position presents at this line or goes to the right hand approaching the Si peak, the GaP crystal of the epilayer will then shrink perpendicularly while expands horizontally, and finally shows a tensile strain (relaxed). Second, when the peak shifts away to the left hand of the dashed line, the crystal will expand perpendicularly, and shows a compressive strain relative to the GaP bulk. Therefore, the layer would either be relaxed or strained. Accordingly, the epilayer of the sample S1:1846 exhibits the biggest tensile strain, because its peak is the closest to the Si peak, resulting in the smallest perpendicular

lattice parameter (Table 5.1). But, the tensile strain decreases in the sample S2:1848, and transformers to a compressive strain in the sample S3:1849. That means, the epilayers of the samples S1:1846 and S2:1848 are relaxed while it is a bit strained in the sample S3:1849.

In order to enhance this finding, SEM images of these films are compared. Shown in Fig. 5.2 are the SEM images of the GaP surface morphology and the interfaces of theses samples. The nominal thicknesses of the epilayers of these samples, listed in Table 5.1, were measured from these images. The surface morphology images confirm that both samples S1:1846 and S3:1849 (Fig. 5.2(a, e)) exhibit rougher surfaces than the sample S2:1848 (Fig. 5.2(c)).

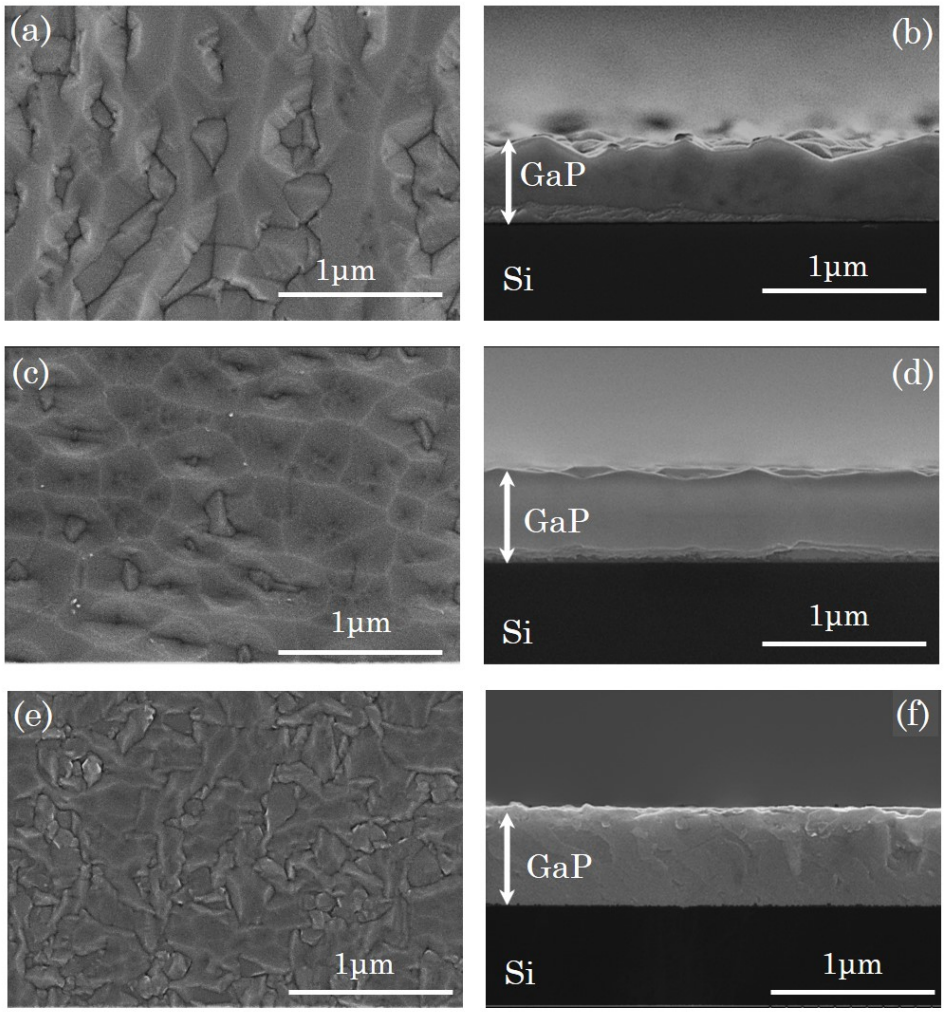

Figure 5.2: *SEM images of the surface morphology and the interface of the GaP/Si samples S1:1846 (a, b), S2:1848 (c, d) and S3:1849 (e, f).*

Furthermore, although the epilayer grown at higher temperature (S1:1846) points to a better quality than the other samples, according to XRD curves, its surface is very rough. This could arise due to increase of GaP grain size with higher temperature [Bi-96].

According to these results, it was deduced that neither lower growth temperature nor higher temperature were appropriate for the growth of high quality GaP epilayer, and consequently, 400 °C could be considered an optimal growth temperature.

5.2.1 Effect of Thermal Annealing

A number of thermal annealing attempts were experienced on the samples grown at 400 °C, starting from this temperature. Besides that, despite the samples grown at 250 °C showed a bad quality, these samples were also processed thermally as attempts to improve their crystal quality. For simplicity, we will refer to the annealing of the samples grown at 400 °C by (A), and for the samples grown at 250 °C by (B) in the subsections below.

5.2.1.1 Thermal Annealing (A)

For the samples grown at 400 °C, the thermal annealing process was initiated starting from this temperature. Some of GaP/Si films were grown with identical growth conditions, while they were annealed with different conditions. Table 5.2 demonstrates growth conditions for three samples: S4:1893, S5:1892 and S6:1903.

Sample No.	T_g $^\circ C$	Annealing $^\circ C/min$	FWHM (2θ) sec	$m_\perp$ %	$a_\perp$ $^\circ A$	$\varepsilon_\perp$ 10^{-3}
S4:1893	400	400/10	844	0.242 ±0.0012	5.4441 ±0.00006	-1.22 ±0.011
S5:1892	=	500/10	674	0.232 ±0.0006	5.4436 ±0.00003	-1.32 ±0.006
S6:1903	=	(400-480)/90	640	0.392 ±0.0239	5.4523 ±0.00013	0.275 ±0.023

Table 5.2: *Growth conditions of the GaP/Si films S4:1893, S5:1892 and S6:1903. T_g is the growth temperature, FWHM is the full-width at half-maximum, $m_\perp$ is the perpendicular lattice mismatch, $a_\perp$ is the perpendicular lattice parameter of the layer and $\varepsilon_\perp$ is the perpendicular strain of the layer.*

After terminating the growth process, the Ga shutter was closed and immediately followed by thermal annealing under PH_3 flux using two different methods: constant and SGA. The samples S4:1893 and S5:1892 were annealed at certain temperatures

of 400 °C and 500 °C for 10 min, respectively. This type of annealing is called constant. Annealing the sample S6:1903 was carried out by increasing the temperature gradually at a rate of 1.6 °C/min for 50 min, and then it was kept constant for 40 min. This type of annealing is referred to as SGA. This sample was then cooled to room temperature slowly with a rate of 7 °C/min. Figure 5.3 shows a schematic representation for the SGA process and cooling the sample to room temperature conducted on the sample S6:1903.

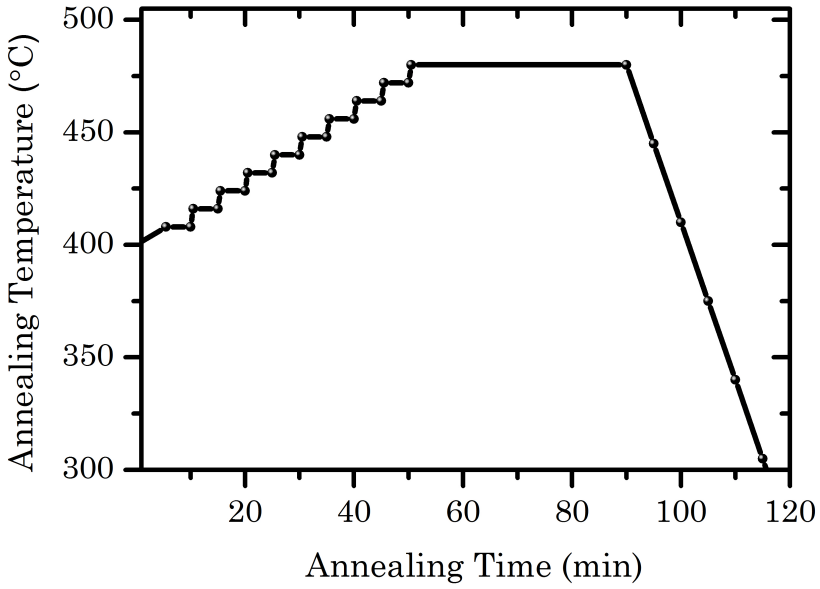

Figure 5.3: *Representation for the step-graded thermal annealing of the GaP/Si heterostructure sample S6:1903. The annealing temperature is raised from 400 to 480 °C by a rate of 1.6 °C/min for 50 min, and then it is kept constant for 40 min. The sample is cooled to room temperature for one hour.*

The GaP epilayer structure was monitored by RHEED throughout the annealing process. In the case of constant annealing, the GaP epilayer exhibited a spotty pattern the entire time of annealing, indicating a rough surface. While in the SGA method, the RHEED pattern was changed with temperature. The RHEED patterns of the sample S6:1903 are shown in Fig 5.4.

At a temperature of 400 °C, the pattern was spotty, and then reconstructed into 2×4 at a temperature of 420 °C (Fig. 5.4(a, b)). The latter remained fixed up to 460 °C (Fig. 5.4(c, d, e)). At 480 °C the reconstructed pattern became sharper (Fig. 5.4(f)), referring to the crystalline quality improvement.

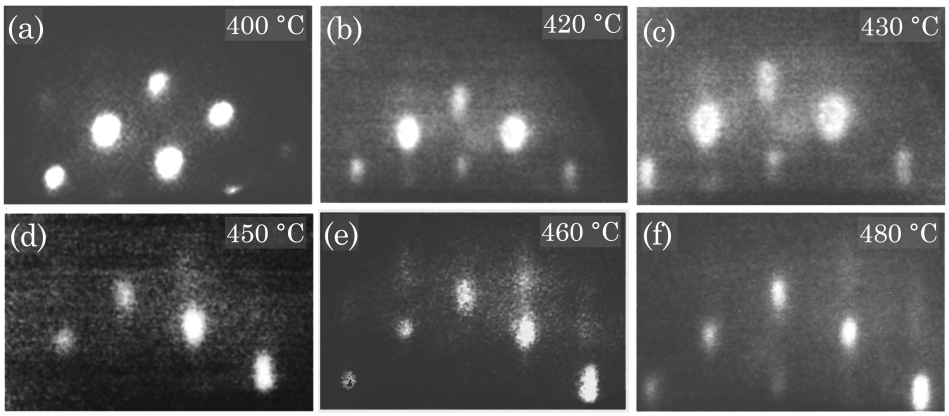

Figure 5.4: *The RHEED pattern reconstruction of the GaP epilayer of the sample S6:1903 that grown at 400 °C. A spotty pattern is seen in (a), while the other patterns show 2×4 reconstruction. A sharper pattern is seen at 480 °C.*

The quality of the annealed GaP/Si films was then evaluated by symmetric XRDs. Figure 5.5 illustrates a comparison for $(\theta/2\theta)$ XRDs of the reflection plane (004) for the samples S4:1893, S5:1892 and S6:1903. This figure clearly shows that the films annealed at constant temperatures are tensile strained, while SGA gives rise to shift the GaP peak away from the Si peak with higher intensity (S6:1903).

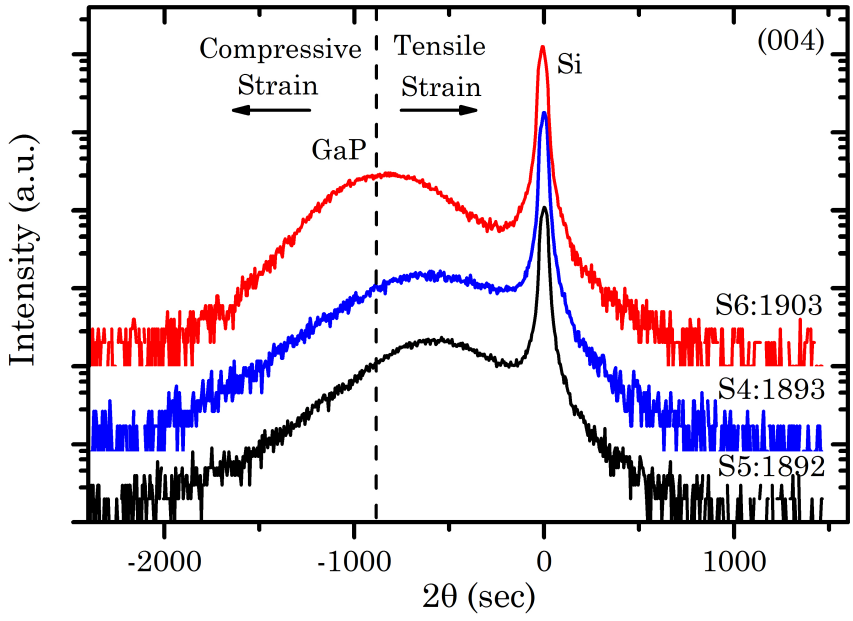

Figure 5.5: *The $(\theta/2\theta)$ XRDs for the annealed GaP/Si films (S4:1893, S5:1892 and S6:1903) grown at 400 °C. The samples S4:1893 and S5:1892 were annealed at 400 °C/10 min and 500 °C/10 min, respectively. The sample S6:1903 was annealed by SGA method at 400-480 °C/90 min.*

However, the epilayer of the last sample does not show a compressive strain.

Obviously, due to this annealing, the GaP peak of the sample S6:1903 is less broadened in comparison with those of the samples S4:1893 and S5:1892, confirming the reduction of the dislocation density, which is calculated by:

$$N = \frac{\beta^2}{9b^2}, \tag{5.1}$$

where β is FWHM of XRDs peak, measured in radian, and b is the Burger's vector, which is equal to (a/2)[110], with a being the lattice parameter of GaP. The values of N for the samples S4:1893 and S6:1903 are determined to be 3.12 $\times 10^8$ and 1.79 $\times 10^8 cm^{-2}$, respectively. As a result, the dislocation density of the film annealed with the SGA method is approximately reduced by a factor of 1.74 compared to that annealed at a constant temperature.

The surface morphology and the interface of the GaP/Si heterostructure SEM images of these samples are shown in Fig. 5.6.

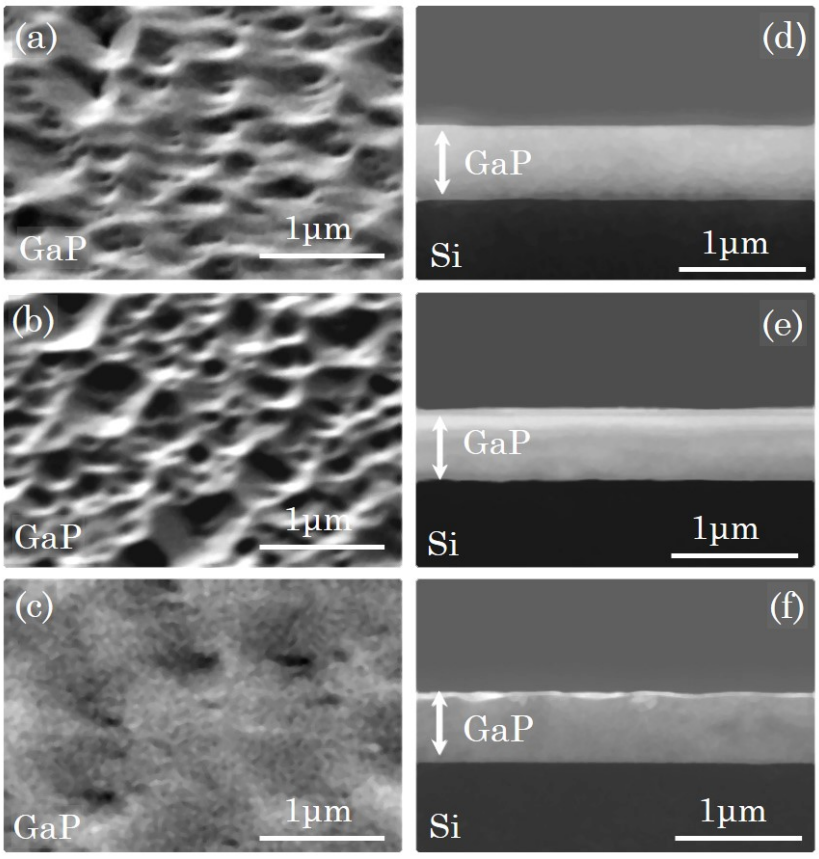

Figure 5.6: *SEM images of the surface morphology and the interface of the GaP/Si samples S4:1893 (a, d), S5:1892 (b, e) and S6:1903 (c, f) grown at a temperature of 400 °C.*

The nominal thickness of the epilayers is 0.49 μm as measured from these images. Due to annealing, they exhibit different surface morphologies, and the smoothest surface is correlated to SGA sample (Fig. 5.6(c)).

5.2.1.2 Thermal Annealing (B)

As the epilayer grown at the lower temperature showed a compressive strain (S3:1849), while this temperature resulted in a bad-crystalline quality layer (S3:1849), the crystal quality was attempted to be improved via thermal annealing. For this reason, the effect of thermal annealing on the structural properties of some of GaP/Si samples grown at a temperature of 250 °C was studied. In Table 5.3, the growth conditions for the GaP/Si samples S7:1887, S8:1886 and S9:1902, grown at this temperature, are listed.

Sample No.	Annealing $^{\circ}C/min$	FWHM (2θ) sec	$m_{\perp}$ %	$a_{\perp}$ $^{\circ}A$	$\varepsilon_{\perp}$ 10^{-3}	N (10^8) cm^{-2}
S7:1887	400/10	1142	0.413 $\pm$0.0025	5.4535 $\pm$0.00014	0.495 $\pm$0.026	5.73
S8:1886	500/10	1486	0.420 $\pm$0.0013	5.4539 $\pm$0.00007	0.568 $\pm$0.014	9.7
S9:1902	(400-480)/90	917	0.374 $\pm$0.0015	5.4515 $\pm$0.0051	0.110 $\pm$0.009	3.69

Table 5.3: *Growth conditions of the GaP/Si films S7:1887, S8:1886 and S9:1902. All the samples were grown at T_g of 250 °C, FWHM is the full-width at half-maximum, $m_{\perp}$ is the perpendicular lattice mismatch, $a_{\perp}$ is the perpendicular lattice parameter of the layer, $\varepsilon_{\perp}$ is the perpendicular strain of the layer and N is the dislocation density of the heterostructures.*

In these samples, the thermal annealing was carried out in the same manner that used in the former samples. The $\theta/2\theta$ XRDs of the reflection plane (004) for these samples are shown in Fig. 5.7. This figure shows that all the GaP epilayers show a compressive strain. On the other hand, as the epilayer peaks of the first two samples are analogues, this suggests that the 10 min annealing did not so much impact on the crystal quality. But, due to SGA, the GaP peak of the sample S9:1902 is less broadened, and therefore the dislocation density is much reduced.

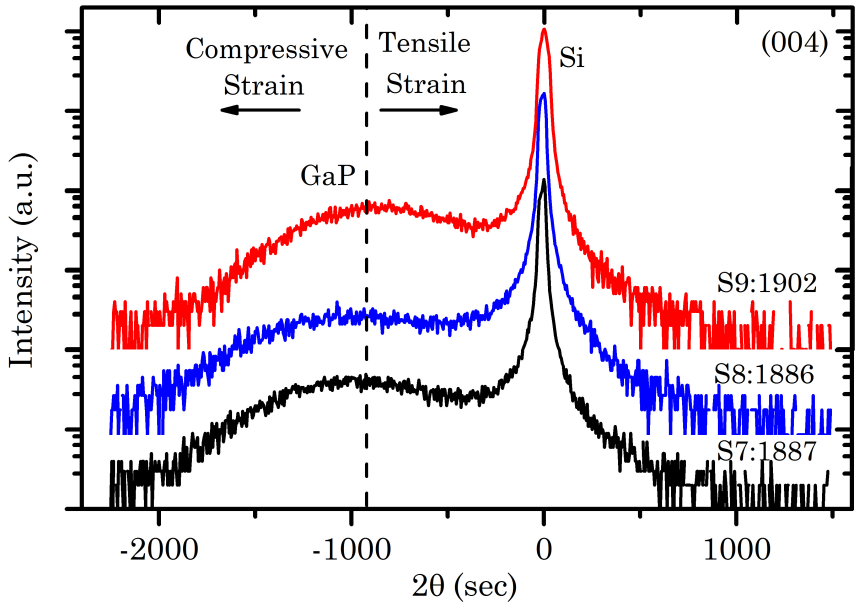

Figure 5.7: *The (θ/2θ) XRDs for the annealed GaP/Si samples S7:1887, S8:1886 and S9:1902 grown at 250 °C. The first two samples were annealed at 400 °C/10 min and 500 °C/10 min, respectively, and the sample S9:1902 was annealed by SGA method at 400-480 °C/90 min.*

Furthermore, Fig. 5.8 illustrates the SEM images of the surface morphologies of the samples S8:1886 and S9:1902. Obviously, an improvement in the GaP crystal quality of the SGA sample arises.

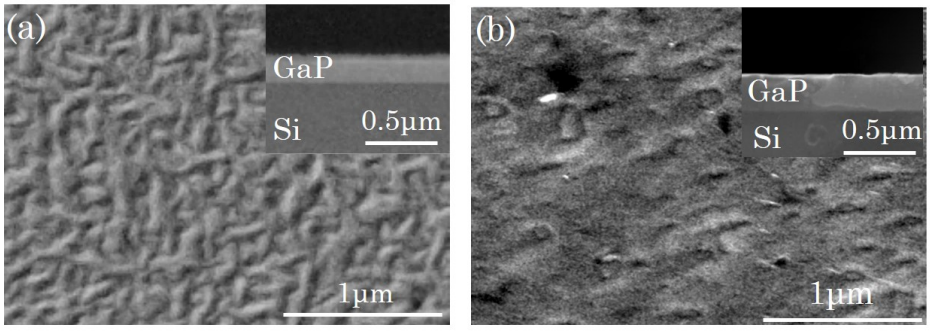

Figure 5.8: *The surface morphology images of the samples (a) S8:1886 and (b) S9:1902. Each inset image shows the GaP/Si interface.*

This finding was also confirmed via AFM images. Figure 5.9 illustrates the AFM images for the surfaces of the samples S8:1886 and S9:1902, in which the root-mean square (RMS) values are measured to be 3.5 nm and 3.37 nm, respectively.

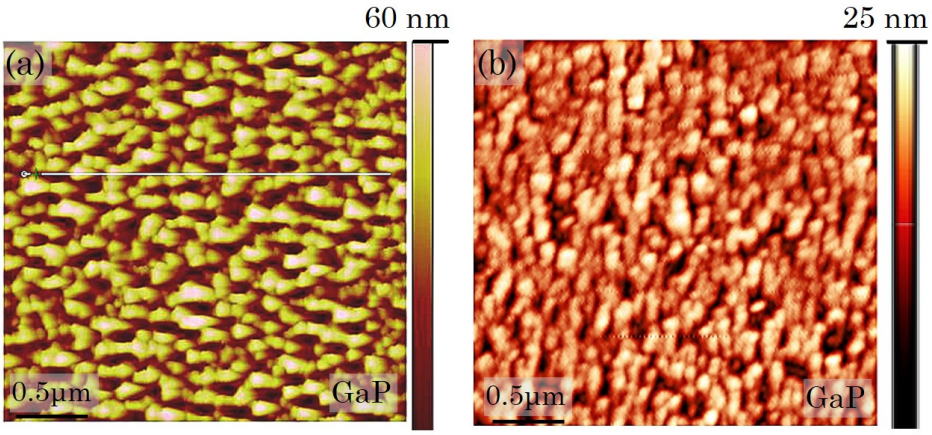

Figure 5.9: *AFM images for the surface morphologies of the samples (a) S8:1886 and (b) S9:1902. The RMS values of these samples are 3.5 nm and 3.37 nm, respectively.*

5.3 Effect of Epilayer Thickness

The critical thickness for GaP/Si is estimated according to the Matthews and Blakeslee model [Mat-74], using Eq. 2.9. For a single epilayer with only one interface the equation is modified as below [Nam-98]:

$$h_c = \frac{b}{4\pi f}\left(\frac{1-\nu/4}{1+\nu}\right)\left(\ln\frac{h_c}{b}+1\right), \tag{5.2}$$

where $\nu = c_{12}/(c_{12}+c_{11})$ with c_{11} and c_{12} are the elastic constants of GaP, which are equal to 14.05×10^6 N/cm^2 and 6.203×10^6 N/cm^2, respectively [Ada-09]. Substituting these values in Eq. 5.2 gives a critical thickness about 315 A° for GaP/Si, (where the Burger's vector b = 3.85 °A).

Since the quality of the epilayer is highly related to the thickness, different thicknesses of the GaP layers were experienced to reach the optimal case. Table 5.4 contains the growth conditions for two GaP/Si films having different thickness and compared with the results obtained for the sample S6:1903, since they were grown and annealed similarly.

The annealing time for the samples S10:1905 and S11:1904 is less than that of samples S6:1903. This was conducted in such a way, because the surface reconstruction remains constantly under the influence of just 50 min annealing, as has already been seen in Sec. 5.2.1.1.

Sample No.	T_g $^\circ C$	h nm	Annealing $^\circ C/min$	FWHM (2θ) sec	N (10^8) $10^8, cm^{-2}$
S10:1905	400	351	(400-480)/60	669	1.96
S11:1904	=	188	(400-480)/60	944	3.91

Table 5.4: *Growth conditions of the GaP/Si films S10:1905 and S11:1904. T_g is the growth temperature, FWHM is the full-width at half-maximum and N is the dislocation density.*

The thicknesses of all the samples are thus much larger than the critical thickness. Their $\theta/2\theta$ XRDs for reflection plane (004) are compared in Fig. 5.10. Evidently, when the layer thickness increases, the GaP peak shows higher intensity and smaller FWHM, which corresponds to the sample S6:1903.

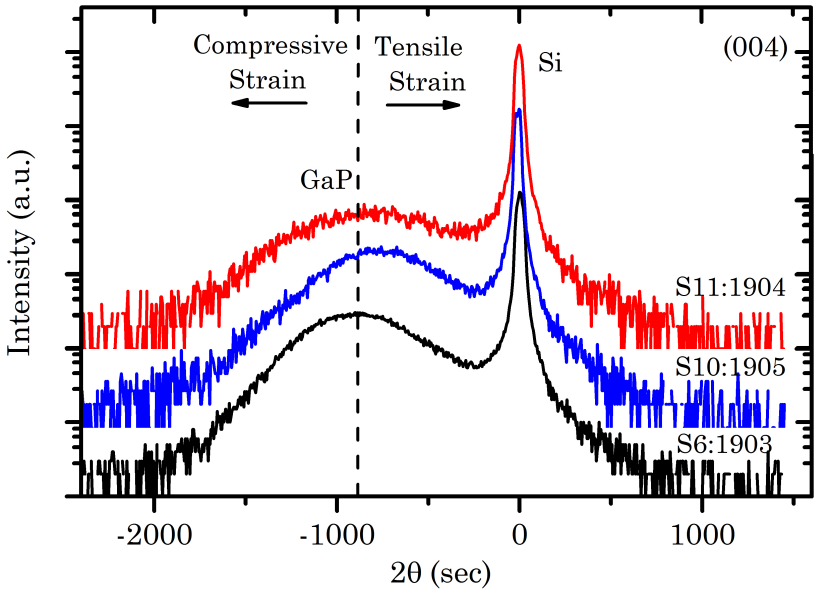

Figure 5.10: *The $(\theta/2\theta)$ XRDs for the annealed GaP/Si samples S6:1903, S10:1905 and S11:1904 grown at 400 $^\circ C$ with thicknesses of 495, 351 and 188 nm, respectively. The peak intensity increases as the thickness increases.*

The SEM images of these samples are shown in Fig. 5.11 and Fig. 5.6(c, f). These results confirm that the sample S6:1903 still has a better quality layer relative to both samples.

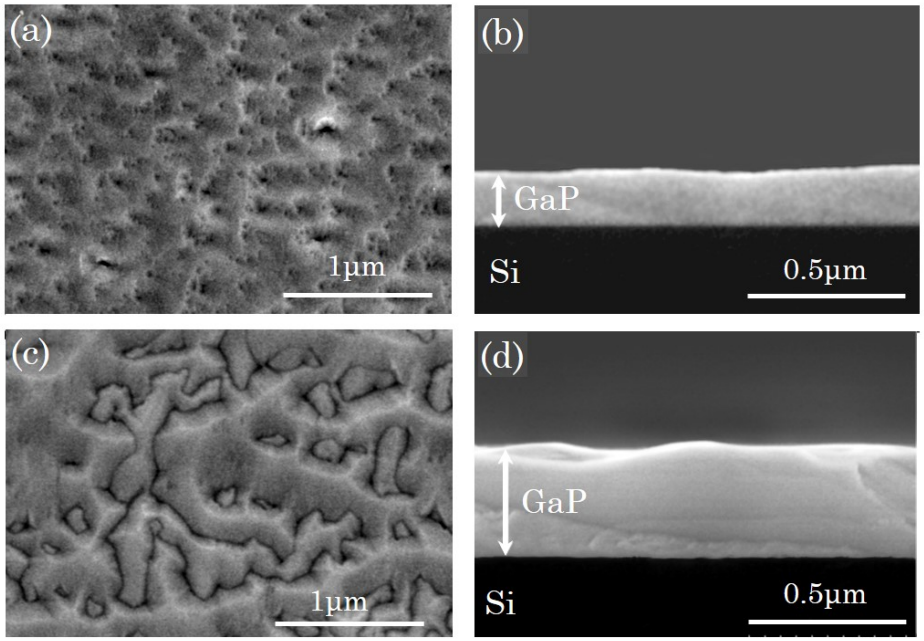

Figure 5.11: *SEM images of the surface morphology and the interface of the GaP/Si heterostructure sample S11:1904 (a, b) and the sample S10:1905 (c, d).*

Also, the AFM images for the samples S6:1903, S10:1905 and S11:1904 are shown in Fig. 5.12, by which the values of RMS are found to be 7.7, 6.2 and 12.4 nm, respectively. It is seen that the surface of the thinner layer is somewhat smooth,

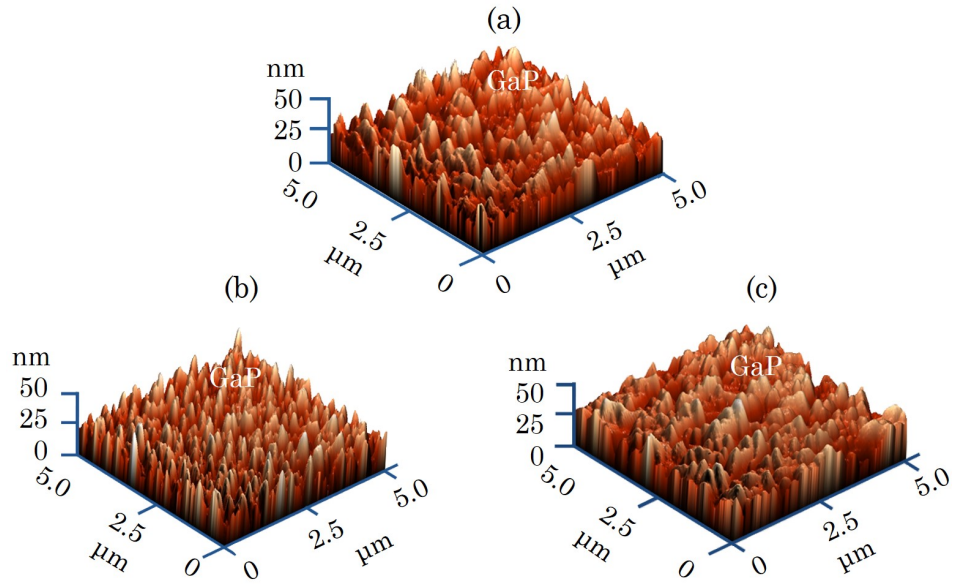

Figure 5.12: *AFM images of the surface morphology of the GaP/Si sample S6:1903 (a), sample S11:1904 (b) and sample S10:1905 (c).*

but its FWHM value is larger. By increasing the thickness (S10:1905) the surface becomes rougher because the island size increases, while FWHM is decreased. Thus, the improvement of the surface morphology after increasing the layer thickness suggests that the incoming GaP atoms may diffuse among the islands and coalesce during annealing.

5.4 Mosaicity and Tilt in the GaP Layer

So far the study is focused on the out-of-plane crystal structure. Further explanation about the effect of the growth conditions on the crystal quality can be recognized via asymmetric XRDs. Grazing incidence and grazing exit ($\omega/2\theta$) scans for reflection planes 224, 115 and 044 were achieved at different azimuthal rotation. Then, the recoded data were converted to RSMs using Eq. 4.9 and Eq. 4.10. A visualization of the GaP crystal structure is represented in Fig. 5.13. In this figure, RSMs of the reflection planes (224) for the unannealed sample S3:1849 and the annealed sample S7:1887 are presented.

In the map of sample S3:1849, high diffuse scattered intensity in the GaP peak along Q_x is observed, indicating that the layer is of a mosaicity nature. This leads to tilt the lattice from the surface normal [Mes-95]. Since the formation of dislocations leads to tilt the region surrounding the lattice, the layer would exhibit a mosaic spread. As shown in Fig. 5.13(b), the diffuse scattering in the layer of the sample S7:1887 is decreased, which refers to a lower mosaicity.

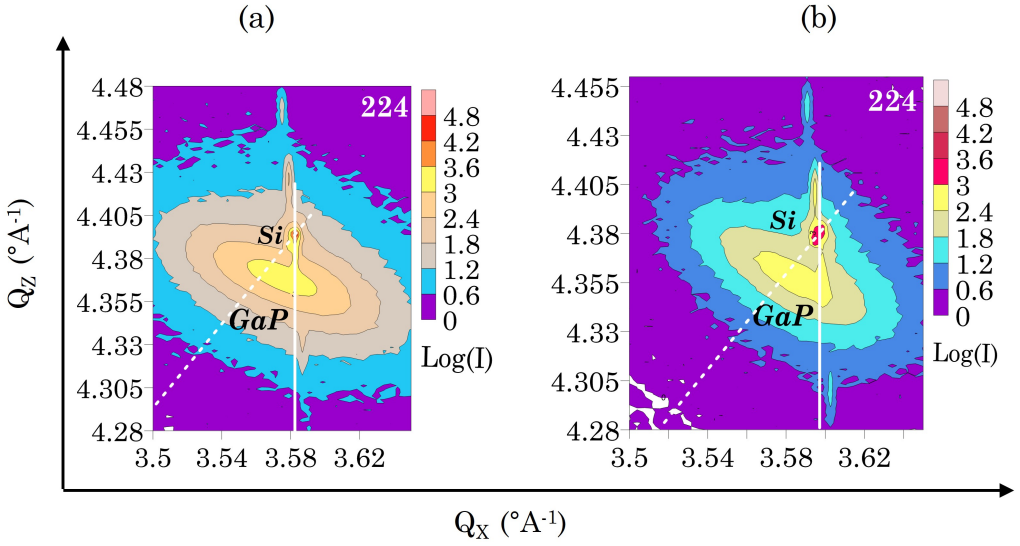

Figure 5.13: *Reciprocal space maps for the GaP/Si sample S3:1849 (a) and sample S7:1887 (b) for reflection plane 224. Higher mosaicity is seen in map of the sample S3:1849. The data of these RSMs were measured with the assistance of Dr. Peter Schäfer/Humboldt-University in Berlin.*

The higher mosaicity is thus correlated to the layer of higher dislocation density, i.e. (S3:1849). But due to annealing, the dislocations decrease and the mosaicity also decreases in the sample S7:1887.

From these RSMs, the values of $m_{\parallel}$ for the GaP crystals of the samples S3:1849 and S7:1887 are found to be - 0.22 ± 0.0013 % and - 0.28 ± 0.0025 %, as well as $\varepsilon_{\parallel}$ were found to be (- 2.75 ± 0.23) $\times 10^{-4}$ and (- 0.78 ± 0.025) $\times 10^{-4}$, respectively. That is, the GaP crystals of both samples are slightly strained compared to the bulk GaP, and more strain occurs in the sample S3:1849.

In addition, although the GaP epilayer is much improved by using SGA, the epilayer may exhibit a mosaicity or tilt as long as there exist crystalline defects. Figure 5.14 shows RSMs of the reflection planes (224) for sample S6:1903. It is evident that the mosaicity in the epilayer of this film is decreased in comparison to that seen in Fig. 5.13. However, the tilt angle caused by the mosaicity can experimentally be calculated using the below equation:

$$\alpha_L = \frac{\Delta\theta_0 - \Delta\theta_{180}}{2}, \tag{5.3}$$

where $\Delta\theta_0$ and $\Delta\theta_{180}$ are the angular splitting between the layer and the substrate peaks in $\omega/2\theta$ scan for 004 reflection plane, measured in the opposite directions; [110] and [-1-10], respectively.

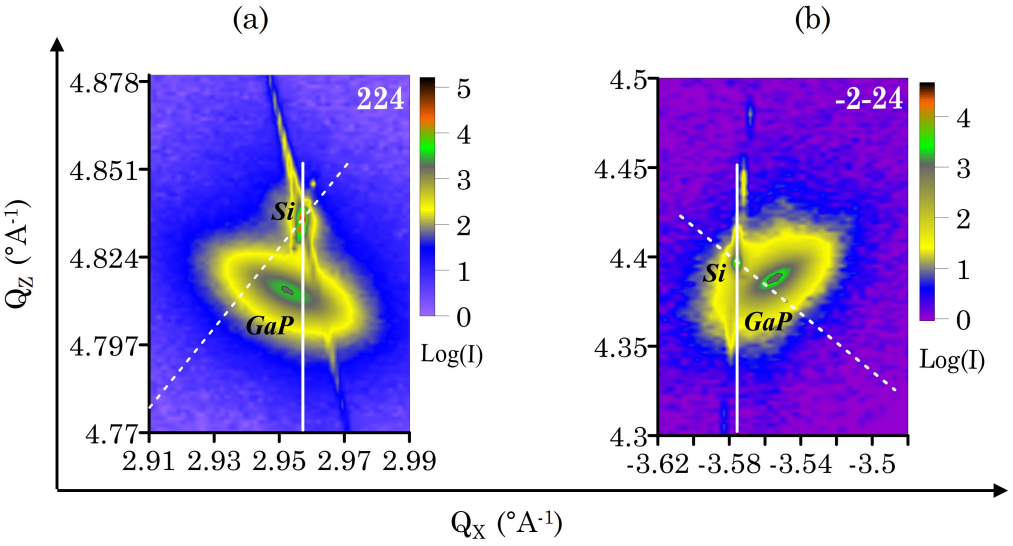

Figure 5.14: *Reciprocal space maps for the GaP/Si sample S6:1903 for reflection planes 224 and -2-24. The data of RSMs were measured with the assistance of Dr. Peter Schäfer/Humboldt-University in Berlin.*

The $\omega/2\theta$ scans of the reflection plane (004) in the directions [110] and [-1-10] for the sample S6:1903 are illustrated in Fig. 5.15. From these measurements, the

tilt angle of the GaP epilayer of the sample is estimated to be 0.0139 °. The tilt occurred in the GaP epilayer may be caused by misorientation of the Si substrate, the dislocations formed during relaxation [Lok-12] or both of them.

Regarding the misorientation of the substrate, it is clearly seen in Fig. 5.15 that the positions of the Si peaks are different and hence there is a difference in the position of the GaP peaks. Therefore, the tilt due to miscut in Si might be added the tilt of the layer due to dislocations.

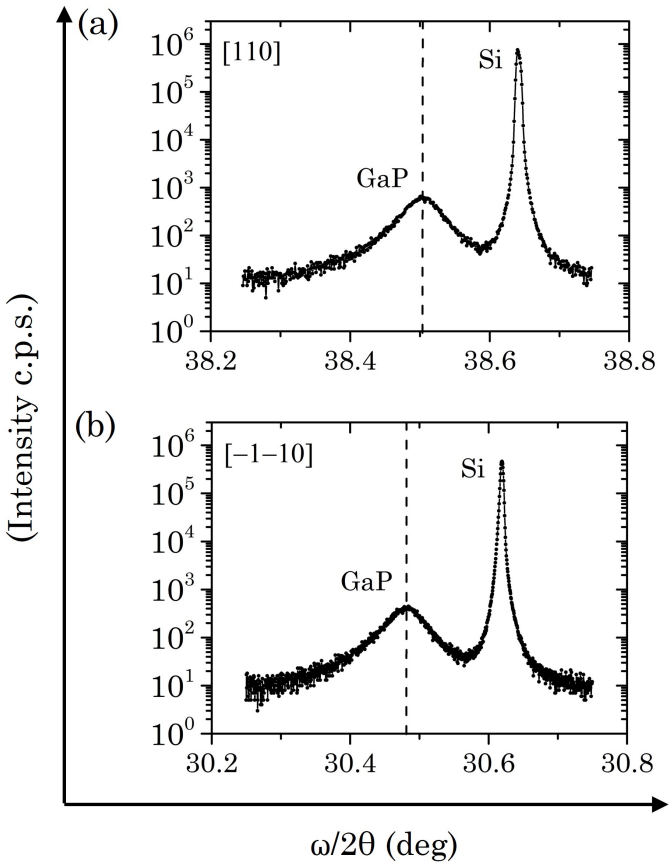

Figure 5.15: *The $\omega/2\theta$ XRD scans for the GaP/Si sample S6:1903 for (004) reflection in the direction (a): [110] and (b): [-1-10]. From these curves, the tilt angle of the GaP epilayer is estimated to be 0.0139 °.*

In addition, further information about this epilayer was obtained by asymmetric XRDs, shown in Fig. 5.16, for reflection planes (224), (-2-24), (115) and (-1-15). From these measurements, the GaP lattice parameters $a_{\perp}$ and $a_{\parallel}$ of the sample S6:1903 were calculated to be 5.4523 ± 0.00013 and 5.4522 ± 0.0003, and the strain values $\varepsilon_{\perp}$ and $\varepsilon_{\parallel}$ were found to be (2.75 ± 0.23) $\times 10^{-4}$ and (2.56 ± 0.5) $\times 10^{-4}$, respectively. These values give a relaxation degree of 100 %, confirming that the GaP crystal lattice is of a cubic shape with a fully-strain relaxation.

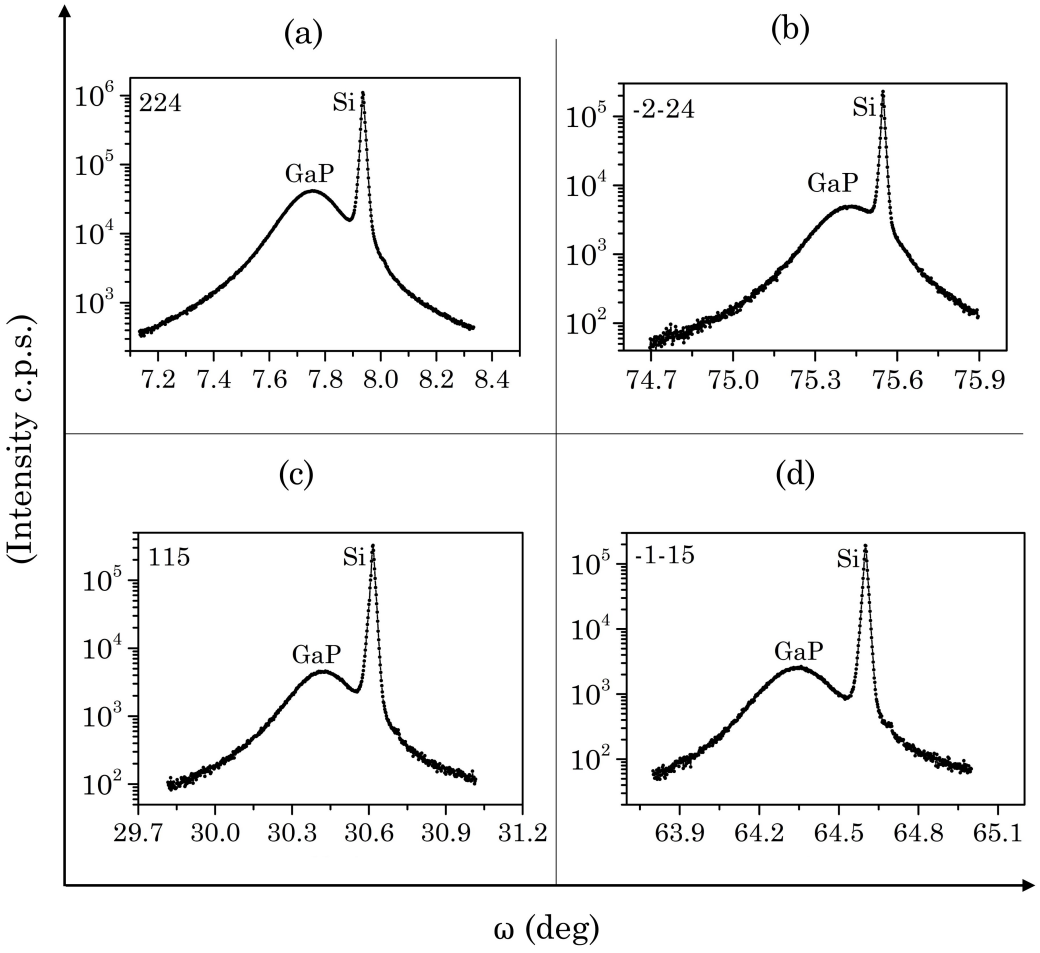

Figure 5.16: *The grazing incidence and grazing exit XRDs of the GaP/Si sample S6:1903 for reflection planes (a):224, (b):-2-24, (c):115 and (d):-1-15.*

5.5 Role of Thermal Expansion Mismatch

Since the GaP/Si system is composed of two semiconductors having different physical properties, the stress in the heterostructure film arises from the mismatch in the lattice parameters together with the mismatch in the coefficients of thermal expansion (CTE). Despite the importance of this issue, a very few studies on the thermal effect on the crystal structure of GaP/Si heterostructure were reported [Dix-06, Yam-10]. Effect of the thermal expansion mismatch on the crystal structure is compared for the samples S5:1892 and S6:1903. These samples were grown with similar conditions except their thermal annealing conditions were different (see Table 5.2). In this comparison, the values of temperature-dependent CTE for GaP and Si were calculated according to the equations presented by Glazov et al [Gla-01] and Watanabe et al [Wat-04], respectively. The thermal strain (ε_{Th}) during annealing,

taking the critical thickness into account, is given by [Jeo-00]:

$$\varepsilon_{Th} = \frac{h_c}{h} \int_{T_g}^{T_a} (\alpha_{GaP} - \alpha_{Si}) dT, \tag{5.4}$$

where T_a is the annealing temperature. When the annealing temperature is increased from T_g (400 °C) to T_a (500 °C) during short time (∼2 min), the strain in the layer at T_g is grew up by an extra amount at T_a due to large ΔT and $\Delta\alpha$. Instead, in the SGA method, because the temperature increases step-by-step, e.g. $T_a = T_g$, $T_a = T_g + 1.6$ °C, ..., the extra thermal strain can be increased gradually, and expressed by summation of all the values of the strain:

$$\varepsilon_{Th} = \frac{h_c}{h} \sum_{T_g}^{T_a} (\alpha_{GaP} - \alpha_{Si}) \Delta T, \tag{5.5}$$

where $\Delta T = 1.6$ °C. That is, the strain due to annealing in the sample S6:1903 increases by small amount every step, because of small difference in CTE and small differential temperature. While, due to the large increase in the thermal strain in sample S5:1892, the strain will be relieved via relaxation the layer during or after annealing immediately. In contrast, because the variation of the strain in the SGA method is very small per a time, there is a probability that the strain resists the relaxation. This suggests that the layer of the sample S6:1903 retains more strain than the sample S5:1892.

On cooling the system to room temperature, the overall residual strain (ε_R) in the film consists of residual lattice mismatch strain (ε_M) and residual thermal mismatch strain. According to the analysis of Dobrynin [Dob-99] the in-plane residual strain can be expressed as:

$$\varepsilon_R = \varepsilon_M + \varepsilon_{Th}, \tag{5.6}$$

where ε_M can be given in terms of the initial lattice mismatch (ε_o) by [Jac-08]:

$$\varepsilon_M = \frac{h_c}{h} \varepsilon_o, \tag{5.7}$$

Substituting Eq. 5.4 and Eq. 5.7 into Eq. 5.6 yields

$$\varepsilon_R = \frac{h_c}{h} \left(\varepsilon_o + \int_{T_a}^{T_r} (\alpha_{GaP} - \alpha_{Si}) dT \right). \tag{5.8}$$

In order to estimate the residual strain for the sample S5:1892, whose thickness, h, is about 490 nm, the values of α_{GaP} and α_{Si} at room temperature are taken to be 2.627×10^{-6} K^{-1} [Wat-04] and 4.7×10^{-6} K^{-1} [Gla-01], respectively. If the layer thickness is firstly assumed to be critical ($h = h_c$), then on cooling the system to room temperature, the residual strain in the epilayer is estimated, using Eq. 5.8, to

be about 2.7×10^{-3}. In this case, the layer is tetragonal distorted, but not coherent-strained, where $\varepsilon_R < \varepsilon_o$ (3.7×10^{-3}). But for the above thickness ($h > h_c$), the residual strain is reduced to 1.7×10^{-4}. Since the last value is much less than that estimated at the critical thickness, the strain in the epilayer must be very small. But the measured value of $\varepsilon_{\parallel}$ for the sample S5:1892 is found to be 1.16×10^{-3}, which is much larger than the estimated value. This implies that the layer is not compressive as well as the negative value of $\varepsilon_{\perp}$ (-1.32×10^{-3}) in Table. 5.2 confirms that the layer is relaxed.

Thus, with increasing the thickness more than critical thickness, the thermal strain increases, so the layer tends to relieve the strain by the generation of misfit dislocations at the interface. As a result, on cooling the layer could either transform from compression to tension or the layer was already tensioned, but then the tension increases.

Since the measured residual strain in sample S6:1903 (2.56×10^{-4}), mentioned in the preceding section (Page-74), is less than that of sample S5:1892, it is reasonably to believe that the relaxation in the last sample was much more than that in the first one before cooling, because the layer has retained more strain due to SGA. Again, during cooling the films both layers start to relax the strain, which is added to the relaxation during annealing. Finally, this gives more relaxation in sample S5:1892, so the (004) XRD of the epilayer of sample S6:1903 shows larger perpendicular lattice constant than that of sample S5:1892 (Fig. 5.5).

5.6 Current-Voltage Characteristics

In the preceding sections, the effect of growth and annealing temperatures on the structural properties of the GaP/Si HS films are reported. Consequently, in order to study the effect of the growth conditions on the transport properties, $I-V$ and $C-V$ measurements are studied. For this purpose, we compare among the samples grown at 400 °C, where their crystalline quality are different. Likewise, since an improvement in the layer quality of the samples grown at 250 °C using SGA method was observed, a comparison of the transport properties for such samples is also presented.

5.6.1 Ohmic and Schottky Contacts

$I-V$ measurements for the GaP layer and the GaP/Si HS were carried out using a computer-controlled Keithely-236 voltage source with a LabView 8.2 software. The experimental setup has already been demonstrated in Sec.4.5.1. In the electrical characterization of semiconductor devices, Ohmic contacts are considered a part of the device resistance. Different materials are usually used for the contacts, such as Al, gold-germanium (Au-Ge) and Ag-paste. Whatever the contact types, it is necessary to keep low resistance and should be stable against temperature change. These factors ensure that the drop voltage due to contacts is as low as possible, and they don't disturb the device performance.

Mostly, the metallic contacts form a Schottky diode with the semiconductor materials. Therefore, Ohmic contacts should be fabricated on the semiconductor so that a rectifying characteristic is avoided. Sumesh et al. [Sum-10] studied the stability of three types of Ohmic contacts including Ag-painted, In-evaporated and fused-In on molybdenum diselenide. They found that the fused-In contacts showed more stability and less resistance after thermal annealing.

The electric contacts used for the heterostructure samples were metallic-In dots of diameter of 0.9 mm annealed on the GaP layer and on the Si substrate under H_2/N_2 gases for 60 sec. Two types of contacts were configured: Schottky contacts for the GaP layer, and Ohmic contacts for both the layer and the Si substrate. A schematic representation for the In-contacts and the SEM image for the contact annealed on the Si substrate are shown in Fig. 5.17. The Schottky contact is necessary to form a Schottky barrier with the GaP epilayer, which was used for capacitance-voltage measurements (Sec. 5.7). Thus, the contacts on the GaP layer enable to characterize the layer only. On the other hand, the GaP/Si film can be characterized using Ohmic contacts on the layer and substrate.

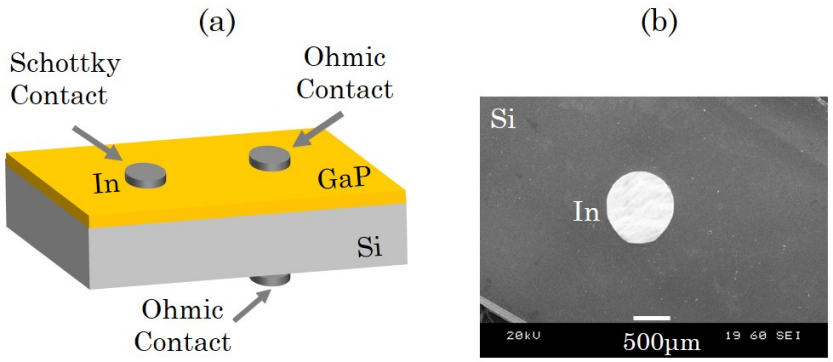

Figure 5.17: *Metallic-In dot contacts on the GaP/Si. (a) Scheme for the contacts: Schottky contact is annealed on the GaP layer while Ohmic contacts are annealed on both the layer and the substrate. (b) SEM image of In dot contact annealed on the Si substrate.*

As illustrated in Fig. 5.18, the optimal annealing temperature for the Ohmic contacts was found to be 350 °C, where the series resistance was found to be minimum at this temperature. Similarly, the optimal temperature for the Schottky contact was found to be 150 °C. The specific ohmic contact resistance (R_c) was measured using two techniques: two-point probe method and parallel geometry. In the first method, a 4 mA current (I) from SMU passes through a GaP strip, with area (A_s)

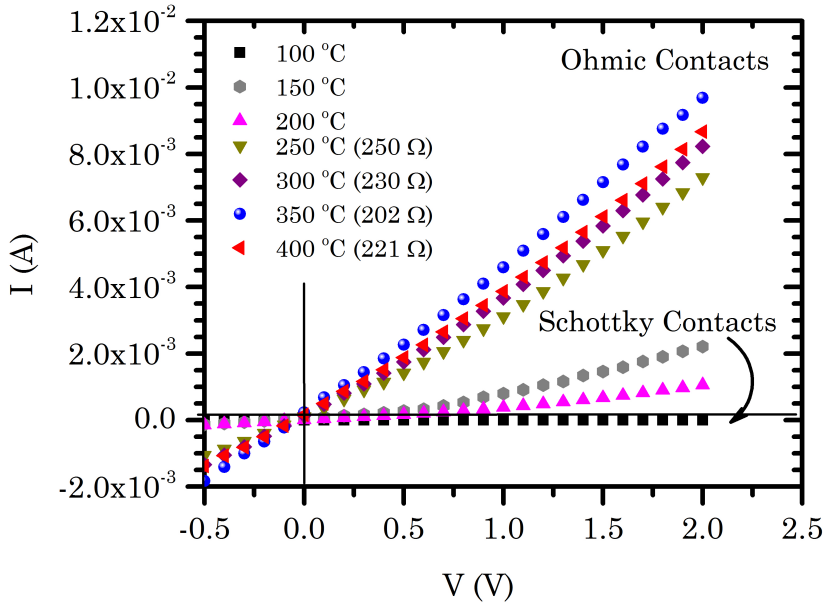

Figure 5.18: *I-V characteristics for the GaP epilayer and GaP/Si sample using In-dot contacts as Ohmic and Schottky contacts. The optimal annealing temperatures for both types of the cantacts are 350 and 150 °C, respectively.*

of 10 × 10 mm^2, and thickness of 0.03 cm. With a separation (L) between the contacts of 10 mm, the current results in a drop voltage (V) of 1.43 V. The contact resistance can be calculated by $R_o = (1/2)(V/I - \rho_b L/A)$, where ρ_b is the resistivity of the bulk semiconductor, which is equal to 10.31 $\Omega.cm$. R_o calculated from this equation was found to be 6.91 Ω. $R_c = R_o A$, with A being the contact area. R_c of the Ohmic contact of the GaP layer was calculated to be 4.35 $\times 10^{-2}$ $\Omega.cm^2$. Similarly, R_c for the contact on the Si substrate was found to be 6.41 $\times 10^{-2}$ $\Omega.cm^2$.

The second method is based on the dependence of the resistance on the separation between two contacts. The separation was chosen to be changed from 2.2 to 8.9 mm, and the corresponding resistance was recorded from $I-V$ plot. The total resistance (R) measured at a given separation is given by [Edw-72]: $R = (1/A)(\rho_c L - 2R_c)$. The plot of R versus L gives the value of R_c, which is estimated for the Ohmic contacts formed on the GaP layer and on the Si substrate to be 3.48 $\times 10^{-2}$ $\Omega.cm^2$ and 4.74 $\times 10^{-2}$ $\Omega.cm^2$, respectively.

5.6.2 I-V Characteristics of the GaP/Si Heterostructure

Figure 5.19 illustrates comparisons between room-temperature $I-V$ characteristics for the samples grown at 250 °C (S3:1849 and S9:1902), as well as for the samples grown at 400 °C (S2:1848, S5:1892, S6:1903 and S11:1904).

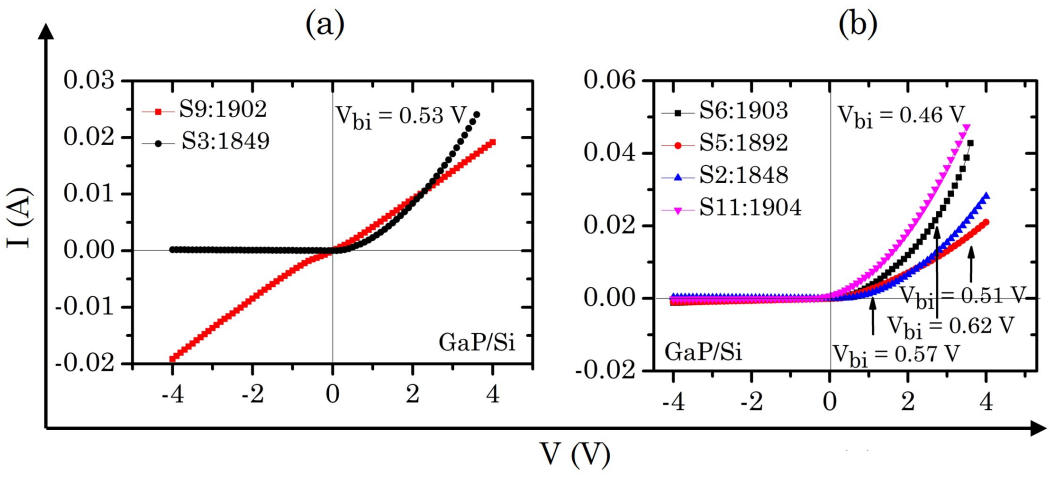

Figure 5.19: *I-V characteristics for the GaP/Si films grown at (a) 250 °C (samples S3:1849 and S9:1902), and at (b) 400 °C (samples S2:1848, S5:1892, S6:1903 and S11:1904). All the samples are annealed except the samples S2:1848 and S3:1849.*

Obviously, all the samples exhibit rectification characteristics, except the sample S3:1849, which has most likely Ohmic resistance. The $I-V$ characteristics were

evaluated depending on the current−voltage relation of a practical diode, in which the current passing through such a device at an absolute temperature T can be given by [Fis-82]:

$$I = I_\circ \left[exp\left(\frac{qV}{\eta kT}\right) - 1 \right], \tag{5.9}$$

where $I_\circ$, V and η are the reverse saturation current, the voltage across the junction and the ideality factor. V is expressed as $V = V_{ap} - IR_s$ with V_{ap} and R_s being the applied voltage and the series resistance of the junction, which is composed of the junction resistance and the contacts resistance. From Fig. 5.19, the built−in voltage values (V_b) were determined to be 0.53, 0.57, 0.51, 0.62 and 0.46 V for the samples S9:1902, S2:1848, S5:1892, S6:1903 and S11:1904, respectively. When V > 3kT/q, Eq. 5.9 reduces to

$$ln(I) = ln(I_\circ) + \frac{qV}{\eta kT}. \tag{5.10}$$

The ideality factor describes the deviation of the experimental $I-V$ characteristics from that of the ideal diode, and expressed using Eq. 5.10 as:

$$\eta = \frac{q}{kT}\left(\frac{\partial(\ln I)}{\partial V}\right)^{-1}. \tag{5.11}$$

The plot of $(\ln I)$ against V is linear, from which the slope gives the value of η, and the intercept on the y-axis at zero voltage gives $I_\circ$. Figure 5.20(a) shows $(\ln I - V)$ plot for the sample S9:1902. The values of η were calculated to be 5.37, 2.88 and 1.86 for the samples S2:1848, S9:1902 and S6:1903, respectively. Also, $I_\circ$ values for these samples were found to be 5.08, 2.35 and 2.99 μA, respectively.

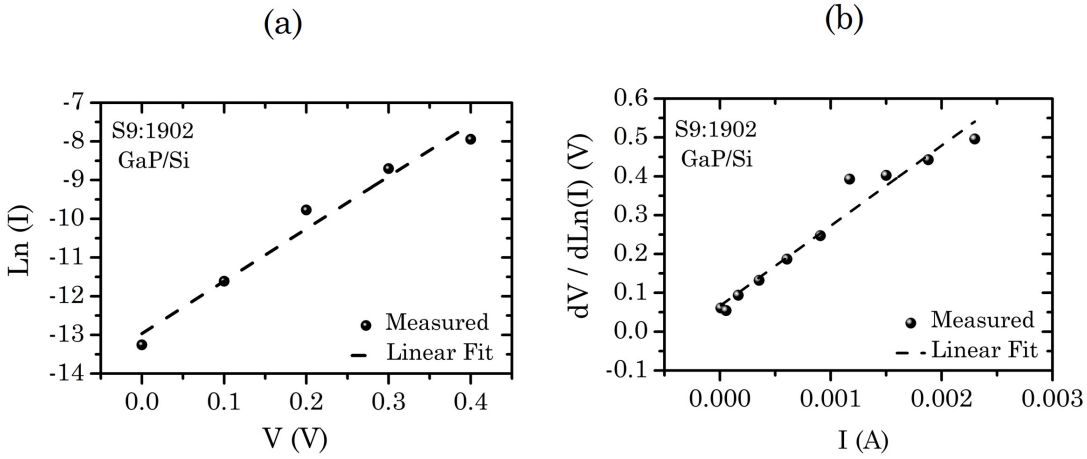

Figure 5.20: *Room-temperature* $\ln(I) - V$ *(a), and* $(dV/d\ln(I)) - I$ *(b) of the GaP/Si film grown at 250 °C (S9:1902).*

This method is widely used for extracting the Schottky and $p-n$ junction diodes parameters [Yue-08, Gho-11]. But, it becomes inaccurate, if the diode has a large series resistance so that it can significantly reduce the forward current, especially at the curvature-forward region of the $I-V$ plot [Gho-11]. With the presence of this parasitic, the voltage across the junction will be reduced because the forward current can be dominated by the series resistance. For this reason, one efficient method used for extracting η and R_s from $I-V$ curve was presented by Cheung and Cheung [Che-86] as below:

$$\frac{dV}{d(\ln I)} = \frac{\eta kT}{q} + IR_s. \tag{5.12}$$

By plotting $(dV/d\ln I)$ versus I, η and R_s can be extracted from the intercept of the line with the y-axis, and the slope of the linear region, respectively. An example of such plot for the sample S9:1902 is demonstrated in Fig. 5.20(b). The values of η for the samples S2:1848, S9:1902 and S6:1903 were determined to be 4.66, 2.16 and 1.74, respectively. The series resistance values for these samples were found to be 206, 227 and 195 Ω, respectively, as well as the Ohmic resistance of the sample S3:1849 was found to be 202 Ω. In addition, the electric conductivities of the heterostructures were calculated using the general formula $\sigma = d/AR_s$, with d and A are the distance between the contacts and the area of the contacts. The values of σ for the samples S2:1848 were estimated to be 0.0338 S/cm, with d and A of 4.0056×10^{-2} cm and 0.00636 cm^2. Likewise, σ for the samples S9:1902, S6:1903 and S3:1849 were calculated to be 0.0304, 0.0359 and 0.0346 S/cm, respectively.

It is interesting to remark that the ideality factor is much reduced due to annealing, which points to an improvement in the quality of the GaP/Si HS. The deviation of this factor from unity can be attributed to the contribution of series resistance and the existence of defects in the epilayer or in the interface. Therefore, the higher value of the ideality factor could most likely be caused by the existence of generation-recombination centers, such as deep levels in the forbidden band gap, or other defects. The improvement in the quality factor for the annealed samples thus possibly resulted from the disappearance of some defects at the layer or the interface [Nar-94]. Also, since dislocations could produce trap levels [Ere-74], the decrement in the dislocation density due to annealing might lead to reduce the quality factor.

Referring to Fig. 5.19(a), we see that at low growth temperature, the unannealed film does not show diode characteristic in contrast to the annealed film. That means the layer under the influence of annealing became auto-doped. In addition, both samples grown at 400 °C were auto-doped with n-type, as we see later.

5.6.3 Energy-Band Diagram of HJ Diode

The energy-band alignment of the HJ diode is possibly sketched by estimating the band structure parameters. To do that, the positions of the Fermi levels of both Si and GaP can be calculated by:

$$\delta_p = kT \ln(\frac{p}{N_V}), \tag{5.13a}$$

$$\delta_n = kT \ln(\frac{n}{N_C}), \tag{5.13b}$$

where p, n, N_V and N_C are the free holes concentration, the electrons concentration, the effective valence-band density of state of Si and the effective conduction-band density of state of GaP, respectively. The conduction-band offset (ΔE_C) of n-GaP/p-Si HJ can be given by [Wol-89]:

$$\Delta E_C = qV_b - kT \ln \frac{nN_{C,P}}{n_p N_C}, \tag{5.14}$$

where n_p and $N_{C,P}$ are the electron density and the effective conduction-band density of state of Si, respectively. From Eq. 5.14, the valence-band offset of GaP/Si HJ can be calculated by:

$$\Delta E_V = (E_{g(GaP)} - E_{g(Si)}) - \Delta E_C, \tag{5.15}$$

where $E_{g(GaP)}$ and $E_{g(Si)}$ are the energy gaps of GaP and Si, which are 2.26 eV and 1.12 eV, respectively. By using $N_{V(Si)} = 3.1 \times 10^{19}\ cm^{-3}$ [Gre-90], $N_{C(Si)} = 2.82 \times 10^{19}\ cm^{-3}$ and $N_{C(GaP)} = 1.8 \times 10^{19}\ cm^{-3}$, we get $\delta_p = 0.319\ eV$, and the calculated values of δ_n, ΔE_C and ΔE_V are listed in Table 5.5.

Sample No.	δ_n (eV)	ΔE_V (eV)	ΔE_C (eV)
S2:1848	0.238	0.884	0.256
S9:1902	0.263	0.899	0.241
S6:1903	0.226	0.836	0.304

Table 5.5: *Energy-band parameters for the GaP/Si HJ obtained from I-V characteristics. δ_n, ΔE_C and ΔE_V are the position of the Fermi level of the GaP junction, the conduction and valence band discontinuities.*

According to these results, it is possible to plot the energy-band diagram for the GaP/Si HJ. Figure 5.21 shows a schematic representation of such diagram for (a) isolation bulk n-GaP and p-Si, and (b) the corresponding n-GaP/p-Si HJ of the sample S6:1903.

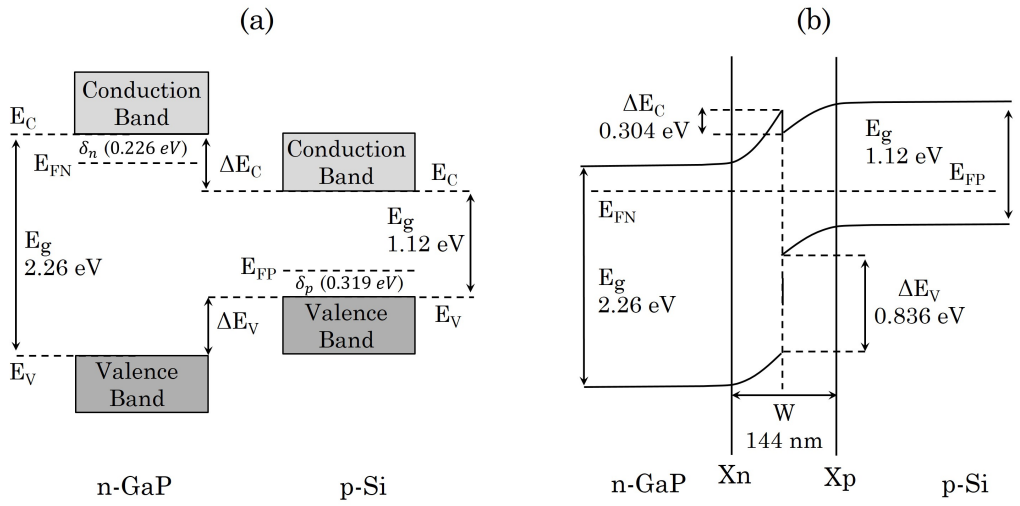

Figure 5.21: *Energy-band diagram of the n-GaP/p-Si HJ diode (sample S6:1903). (a) Isolated Bulk GaP and Si, and (b) the GaP/Si HJ diode. E_g is the energy gap, E_{FN} is the Fermi energy of n-GaP, E_{FP} is the Fermi energy of p-Si, ΔE_C is the conduction band discontinuity, ΔE_V is the valence band discontinuity, δ_n and δ_p are the potions of the Fermi levels in GaP and Si, W is the HJ width, X_n and X_p are the HJ width at n-region and p-region, respectively.*

5.7 Capacitance-Voltage Characteristics

The reverse-bias $C-V$ measurements were carried out in the frequency range from 1 kHz to 1 MHz, at different temperatures in dark using the setup described in Sec. 4.5.2. According to Schottky-Mott equation, the capacitance of Schottky diode can be given by [Sze-07]:

$$C = \sqrt{\frac{qK\epsilon_{\circ}NA^2}{2(V_b - V_{ap} - V_T)}}, \tag{5.16}$$

where K is the dielectric constant of semiconductor material, $\epsilon_{\circ}$ is the vacuum permittivity, N is the carrier concentration, A is the area of the diode, and V_T is the thermal voltage.

5.7.1 C-V Characteristics of the GaP Layers

The room-temperature $C-V$ measurements for the GaP epilayers of the samples S3:1849, S9:1902, S2:1848 and S6:1903, obtained by applying a 50 mV modulation voltage of frequency of 1 MHz from LCR meter, are shown in Fig. 5.22. Clearly, all the epilayers show a capacitive behaviour.

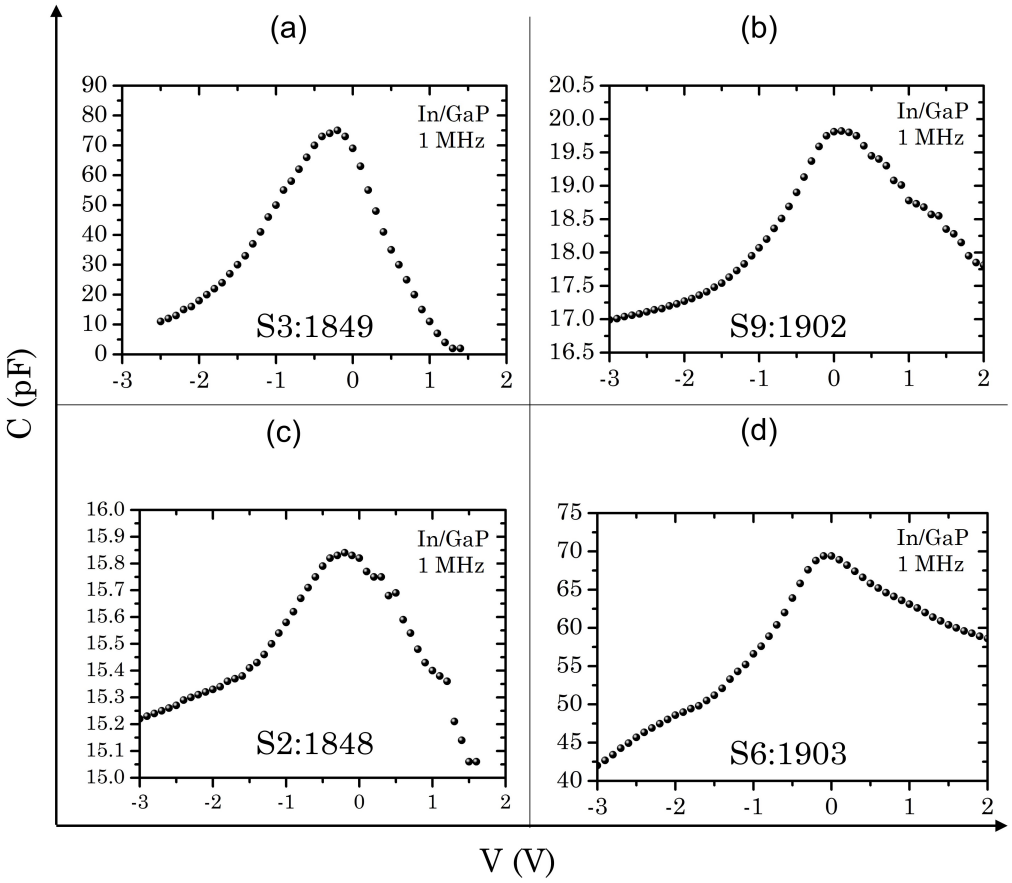

Figure 5.22: *$C-V$ characteristics for the GaP/Si films grown at 250 °C (a and b) and 400 °C (c and d). The samples S2:1848 and S3:1849 were unannealed and the samples S9:1902 and S6:1903 were annealed by step-graded annealing method.*

This type of semiconductor characterization techniques become very useful, when the differential form of Eq. 5.16 respect to V is utilized. In this case the doping concentration N_ω can be obtained by:

$$N_\omega = \frac{-2}{qA^2K\epsilon_o}\left(\frac{1}{d(1/C^2)/dV}\right) \tag{5.17}$$

If N_ω is uniformly distributed throughout the depletion region, the plot of $1/C^2$ versus V should be straight line, with slope proportional to $1/N_\omega$. Figure 5.23 shows $1/C^2-V$ plot obtained over the voltage range from 0 to -2 V for the samples S3:1849, S9:1902, S2:1848 and S6:1903.

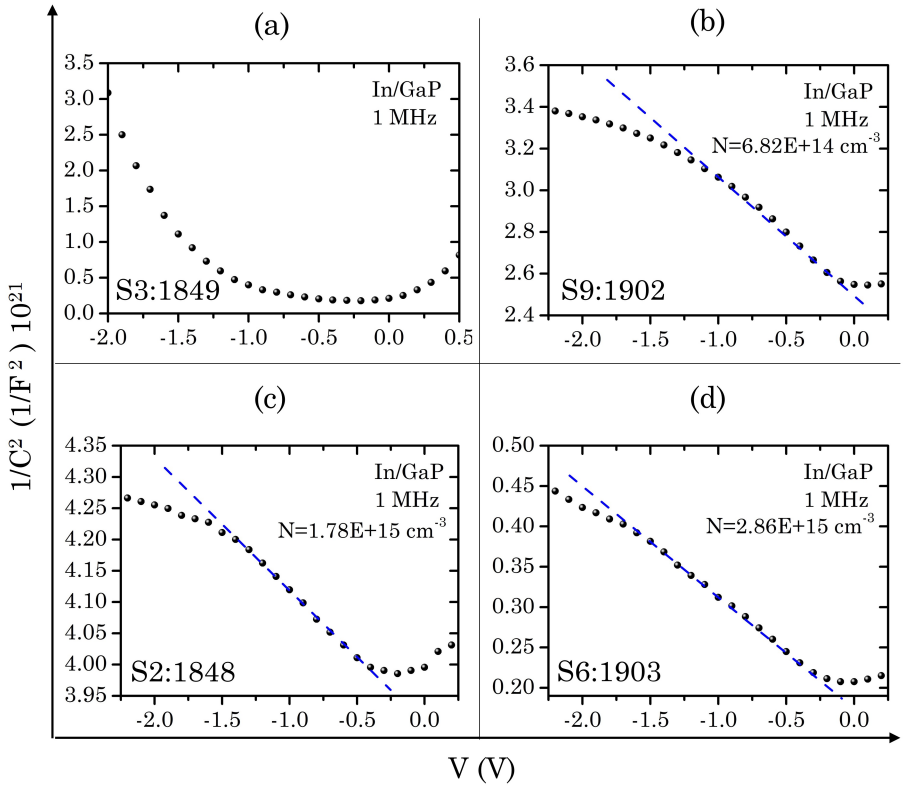

Figure 5.23: *$1/C^2 - V$ characteristics for the GaP epilayers grown at (a and b) 250 °C and at (c and d) 400 °C. The samples S2:1848 and S3:1849 were unannealed and the samples S9:1902 and S6:1903 were annealed by step-graded method.*

In the Schottky diodes, all the samples, except S3:1849, exhibit linear regions with different slopes. From the slope of the linear region with a junction area of 0.00636 cm^2, N_ω could be calculated using Eq. 5.17. The epilayers were found to be n-type, and the values of N_ω were determined to be 1.78 $\times 10^{15}$, 6.82 $\times 10^{14}$ and 2.86 $\times 10^{15}$ cm^{-3} for the samples S2:1848, S9:1902 and S6:1903, respectively.

The $1/C^2 - V$ plot of the sample S3:1849 shows an exponential dependence of $1/C^2$ on V, which means that the charge carrier distribution of the epilayer is non-uniform. On contrary, the epilayers of the other samples are thus auto-doped.

Two possible mechanisms for the auto-doping of the GaP epilayers can be explained on the basis of Azoulay et al. [Azo-89] assumptions. They interpreted that the auto-doping of GaAs layer grown on Si substrate might be caused by exo-diffusion of Si atoms from the substrate to the layer. This is also possible in the GaP epilayer, where Si atoms may diffuse in the layer due to existence of the defect sites in the interface and the layer, forming acceptor or donor. The other most likely reason is the probability of diffusion of phosphorous atoms in the epilayer during annealing

and cooling the film to room temperature. Desorption of phosphorous atoms during annealing is compensated by PH_3 flux, so the reduction of Si on P sites exhibits donor like nature [Dix-08].

5.7.2 Effect of Thermal Annealing on C-V Characteristics

Since we found that the values of N_ω are different for samples S2:1848 and S6:1903, their capacitance values are expected to be different after thermal annealing. Hence, it is interesting to examine the dependence of the measured capacitance on the annealing. Figure 5.24 shows a comparison of $A^2/C^2 - V$ plots for the samples S2:1848, S5:1892 and S6:1903, whose growth conditions are analogous except the annealing methods. (see Table 5.1 and Table 5.2)

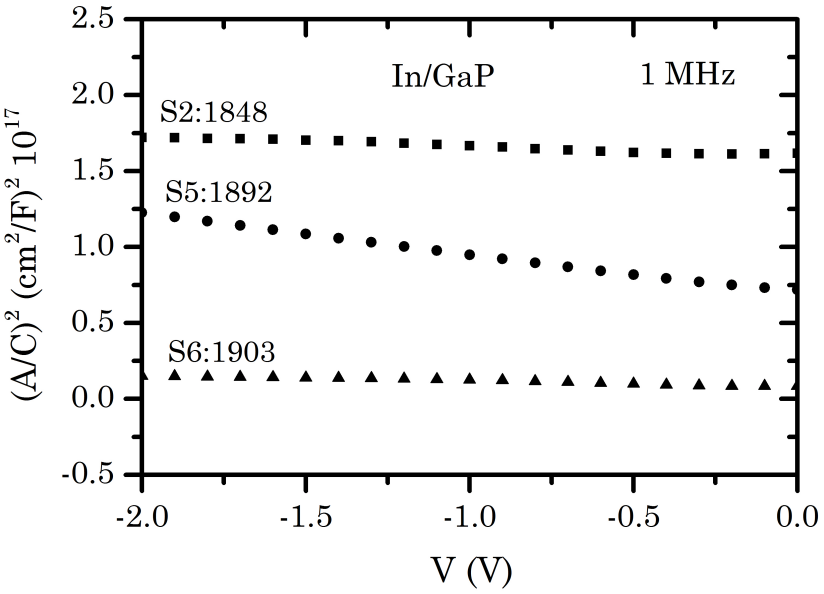

Figure 5.24: *Comparison of $(A/C)^2 - V$ characteristics for the GaP epilayers of the films grown at 400 °C. The sample S2:1848 was unannealed, the samples S5:1892 and S6:1903 were annealed at 500 °C/10 min and 480 °C/90 min, respectively.*

It is seen that the capacitance increases for the annealed film (S5:1892), as well as the capacitance is much increased due to SGA (S6:1903). The similar aspect was also observed for the low temperature epilayers. This finding confirms that the heterojunction depletion width is strongly affected by the annealing. In addition, the dependence of the carrier concentrations of the GaP epilayers on the temperature for the samples grown at 400 °C is shown in Fig. 5.25. The carrier concentration for all the samples decreases at low temperature, and the higher concentration is seen for the SGA sample.

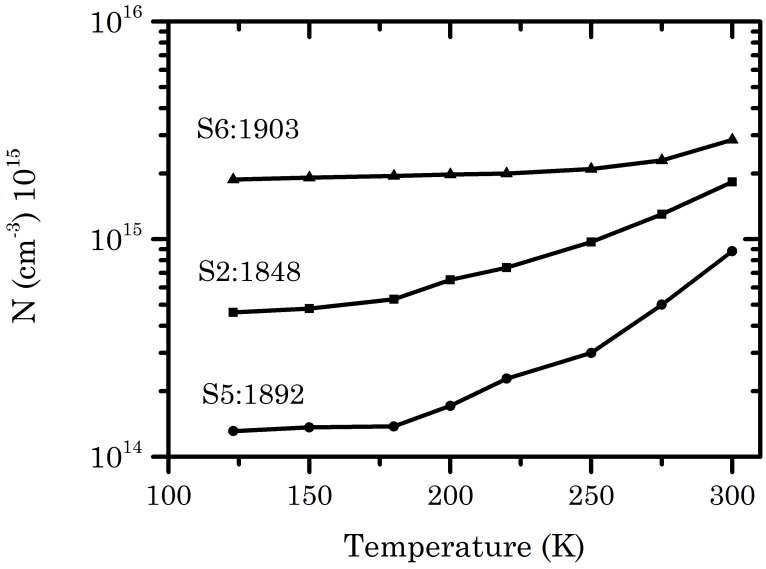

Figure 5.25: *Temperature-dependence of carrier concentrations of the GaP epilayers grown at 400 °C. The sample S2:1848 was unannealed, the samples S5:1892 and S6:1903 were annealed at 500 °C/10 min and 480 °C/90 min, respectively.*

5.7.3 C-V Characteristics of the GaP/Si Heterostructure

The reversed-biased junction capacitance could be represented by a series circuit including the measured capacitance and the series resistance [Glo-73]. Since the use of LCR meter allows to measure the capacitance independent on the series resistance, the effect of the resistance relatively becomes no longer important [Suz-04].

The measured capacitance, however, could strongly be affected by the defects, such as deep levels. Contribution of defects would change the value of the measured capacitance. Figure 5.26 illustrates $1/C^2 - V$ at a modulation voltage frequency of 1 MHz and 1 kHz for the samples S2:1848, S9:1902 and S6:1903.

In Fig. 5.26(a), the linear dependence of $1/C^2$ on V confirms that these samples have abrupt junctions. The measured capacitance at high frequency is limited to the depletion capacitance of the heterojunction without contribution of defects. This implies that defects can not follow the high-frequency modulation voltage. In contrast, the defects can be activated at low-frequency measurements, and their contribution will be added to the junction capacitance causing an increment in the space-charge capacitance [Mak-06]. Therefore, Fig. 5.26(b) shows that the sample S2:1848 exhibits strong-capacitance dependence on the frequency at a forward-bias voltage of 1 V, and weak dependence in the sample S9:1902.

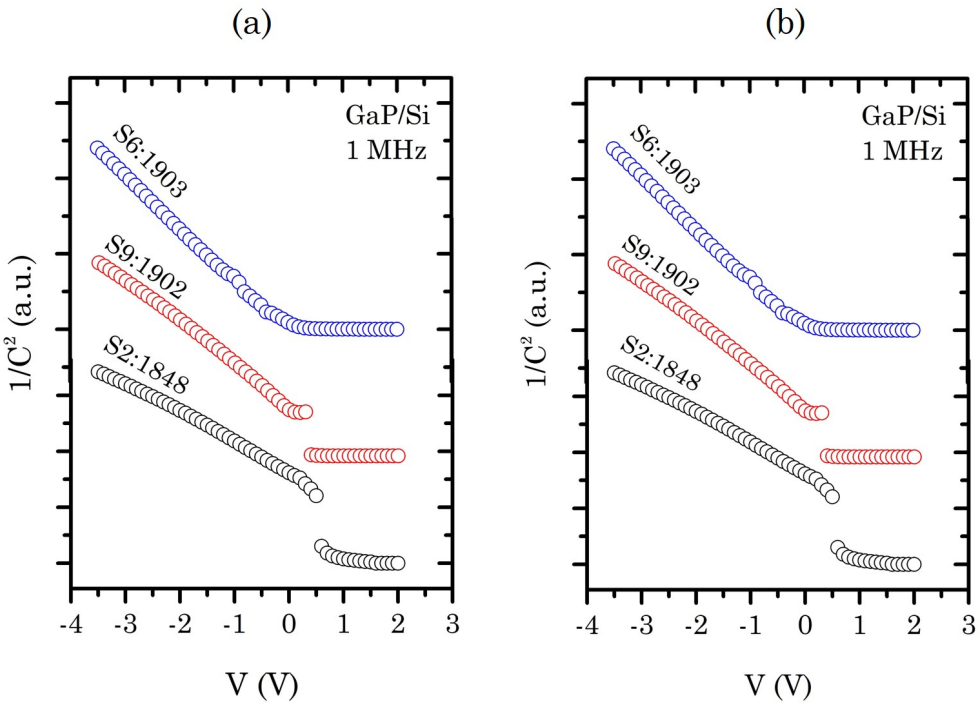

Figure 5.26: $1/C^2 - V$ *characteristics for the GaP/Si films, grown at 250 °C and 400 °C, and measured at frequencies of 1 MHz and 1 kHz. The sample S2:1848 was unannealed, and the samples S9:1902 and S6:1903 were annealed at 480 °C/90 min.*

These measurements are indications to the existence of electrical-activated deep levels at the heterojunction interface. Such levels might be reduced or suppressed by annealing, as seen in the curve of sample S6:1903, where there is no capacitance dependence on the frequency at the forward bias.

Moreover, it has already been stated that the heterojunction depletion width can be impacted by thermal annealing. This because the carrier distribution in the films is different from one sample to another. This deduction can be enhanced via doping profile curve, which represents the variation of the carrier concentration along the depth of the heterojunction, i.e. $(N_\omega - W)$ plot. The depletion layer width of the heterojunction is given, in terms of the measured capacitance, by:

$$W = \frac{\varepsilon_T A}{C}, \tag{5.18}$$

where ε_T is the total permittivity of both the epilayer (ε_1) and the substrate (ε_2), and expressed by $[k_1 k_2/(k_1 + k_2)]\varepsilon_\circ$, with k_1 and k_2 are the dielectric constants of GaP ($k_1 = 9.11$) and Si ($k_2 = 11.7$). The $C - V$ characteristics of HJ can be described by [Sze-07]:

$$\frac{1}{C^2} = \frac{2(V - V_b)}{qA^2\varepsilon_1\varepsilon_2}\left(\frac{\varepsilon_1 N_A + \varepsilon_2 N_D}{N_A N_D}\right), \tag{5.19}$$

where N_A is the acceptor concentration, N_D is the donor concentration. Eq. 5.19 can be reduced to:

$$\frac{1}{C^2} = -\frac{2(V - V_b)}{qA^2\varepsilon_1 N_\omega}, \tag{5.20}$$

where $N_\omega = N_A$ for n^+p (or N_D for p^+n) junction. Thus, for a diode of n^+p, the expression for N_ω obtained from Eq. 5.20 is similar to that expressed in Eq. 5.16. The values of N_ω for the samples S2:1848, S9:1902 and S6:1903, estimated from Fig 5.26(a) using Eq. 5.20, are found to be 7.19 $\times$ 10^{15}, 3.35 $\times$ 10^{15} and 9.37 $\times$ 10^{15} cm^{-3}, respectively.

In light of the above results, the doping profile of the charge carriers for the HS films, $(N_\omega - W)$ plot, can be extrapolated from the $C-V$ measurements using both Eq. 5.19 and Eq. 5.20. Figure 5.27 shows a comparison of the doping profiles for the samples S2:1848, S5:1892, S9:1902 and S6:1903, measured at frequency of 1 MHz.

Obviously, the carrier distributions for all the samples are approximately uniform. But, the annealed samples S9:1902 and S6:1903 show slightly better carrier distributions than that exhibited by the unannealed sample S2:1848 and the annealed sample S5:1892.

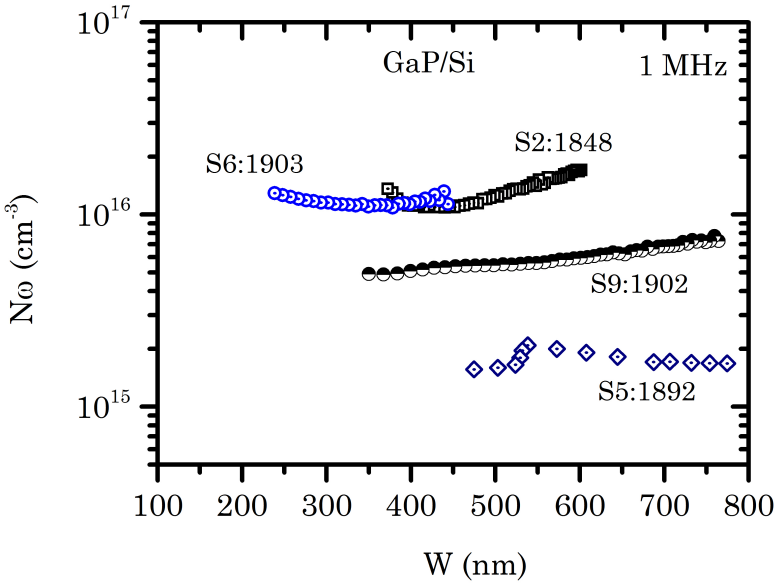

Figure 5.27: *Doping profile of the GaP/Si films grown at 250 °C and 400 °C. The sample S2:1848 was unannealed, the sample S5:1892 was annealed at 500 °C/10 min, and both samples S9:1902 and S6:1903 were annealed at 480 °C/90 min.*

5.8 Low-Frequency Noise Spectroscopy

LFN measurements for the GaP/Si films were achieved in the frequency range from 10 Hz to 100 kHz at the temperature range between 80 and 360 K, using TeachSpin's noise fundamental setup described in Sec 4.6. The block diagram of the electronic circuit used for the noise measurements is shown in Fig. 5.28. By using this circuit the current noise generated in the device under test can be converted to a voltage noise using a current-to-voltage operational amplifier (OP). Both the input resistance (R_{IN}) and the feedback resistance (R_F) were chosen to be 100 kΩ so that the OP amplification gain would be unity, leading to reduce the effect of the OP electronic components. The output noise signal is fed to a band pass filter (BPF) to determine the above frequency bandwidth. Then, the signal is amplified (AMP) as required and measured using a GS-1172 oscilloscope. The time-domain noise signals measured by the oscilloscope could be converted into frequency-domain graph using a mathematical analysis method. An ASCII data of the noise current is fed to a Matlab program, written for implementing a fast Fourier transform using Welch's method, to get the power spectral density (PSD) plot. More details about the analysis are available in Appendix A.1.

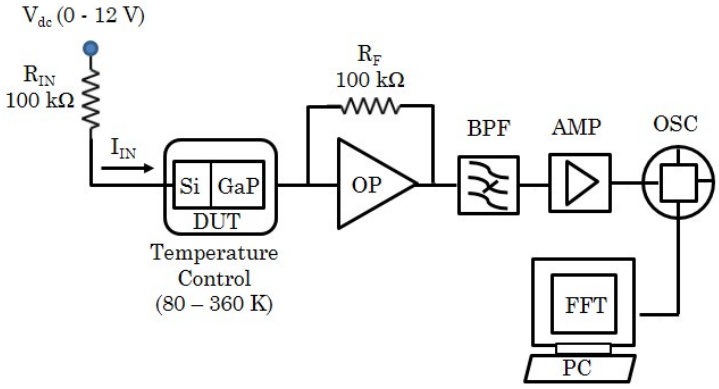

Figure 5.28: *The low-frequency noise measurements setup. The temperature of the GaP/Si film is controlled in the range of 80 - 370 K. OP: operational amplifier, BPF: band pass filter, AMP: amplifier, OSC: oscilloscope and PC: personal computer. The voltage noise is converted to ASCII data and processed using fast Fourier transform.*

Whilst the noise spectral density of the HS films comprises flicker, $G-R$ and thermal noises, the generation of shot noise could be expected as a result of crossing electrons the interface. In such a case, it's quite proper to consider the white noise instead of thermal noise. Hence, all these components are included in Eq. 2.24. By fitting the measured noise spectrum to this equation, the values of $A_{1/f}$ and B_i can be extracted. The analysis method used for extracting these values is somewhat

similar to that reported in Ref. [San-13], and more details about the analysis can be found in Appendix A.1.4.

5.8.1 LFN of the Unannealed GaP/Si Heterostructures

The room-temperature power spectral density of the GaP/Si sample S3:1849 at a bias current of 20 and 100 μA are shown in Fig. 5.29.

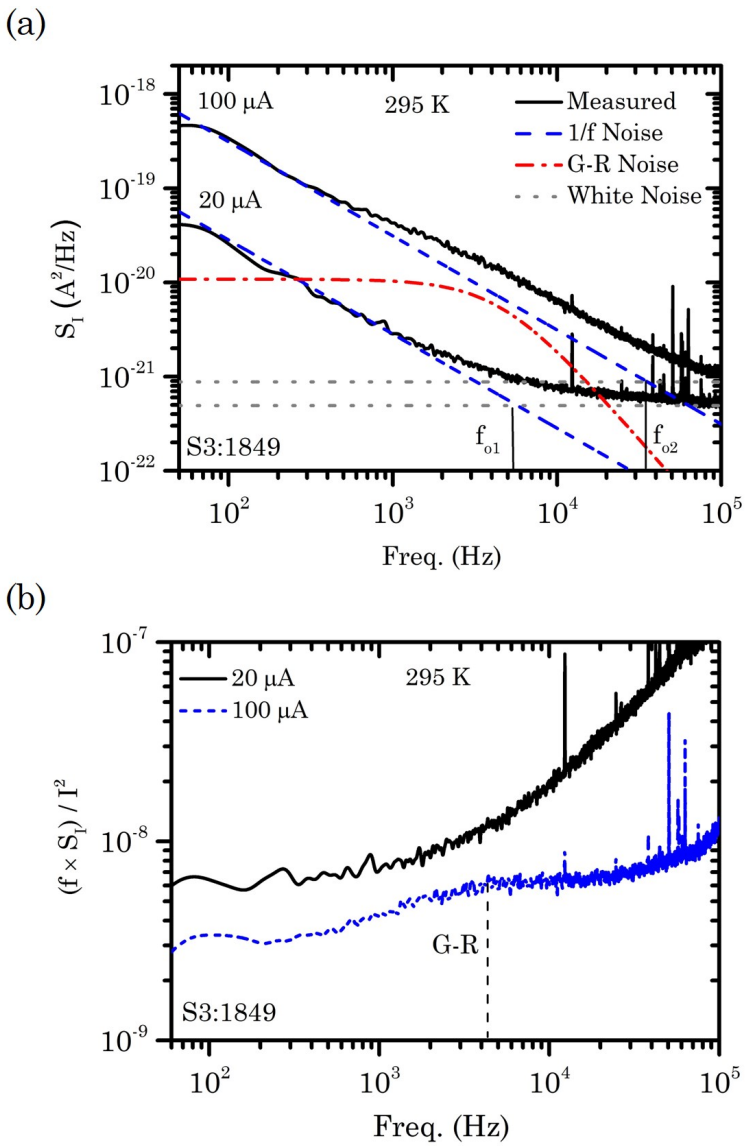

Figure 5.29: *(a) Room-temperature PSD of the GaP/Si sample S3:1849 measured at a bias current of 20 and 100 μA. (b) The normalized PSD plots for the sample at the same bias currents. A $G-R$ noise peak is seen by biasing the GaP/Si diode with a 100 μA current.*

In this figure, one can see the typical LFN characteristics, where the current noise density decreases as the frequency increases down to $1/f$ characteristic frequency ($f_\circ$), and followed by a white noise. The normalized PSD plots, demonstrated in Fig. 5.29(b), depict that Lorentzian peak of $G-R$ noise is not recognized with a bias current of 20 μA, while it presents by increasing the current to 100 μA. It was also found that $G-R$ noise disappeared at the bias currents less than 100 μA. Depending on the normalized PSD plot, the whole spectrum corresponds to 100 μA is extracted to its components: $1/f$ noise, $G-R$ noise at a frequency of 4.2 kHz and white noise.

Since the temperature is a significant parameter that affects on the transport properties of the HS films, the dependence of the noise spectrum on the temperature was studied as well. A comparison of PSD graphs at temperatures of 180 and 240 K is illustrated in Fig. 5.30, in which a $1/f$ line is fully fitted to the spectrum measured at the temperature of 180 K, while a deviation from $1/f$ due to $G-R$ noise formation is seen on cooling the sample to 240 K.

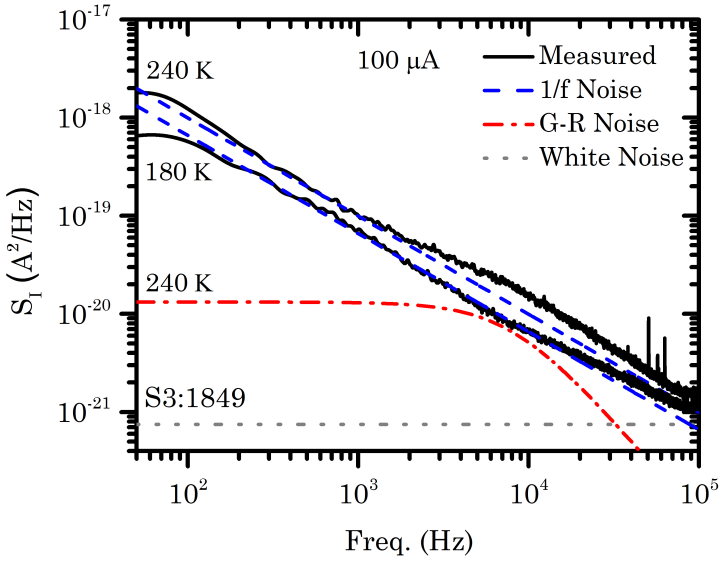

Figure 5.30: *(a) Low-temperature PSD of the GaP/Si sample S3:1849 measured at 240 and 180 K with a bias current of 100 μA. The $G-R$ noise component is seen at the higher temperature.*

The above noise analyses are concerned to the sample grown at 250 °C. On the other hand, since the samples grown at 400 °C show much improvement in their properties, the noise measurements of these samples were therefore intensively analyzed. In the unannealed sample (S2:1848), the PSD measured at room temperature follows a pure $1/f$ noise when the bias current is 10 μA, as shown in Fig. 5.31(a). But, with increasing the current, the $G-R$ noise starts to appear, deviating the

whole spectrum over $1/f$ noise. For instance, at a current of 50 μA, two $G-R$ noise events superimposed over pure $1/f$ noise are clearly seen in Fig. 5.31(b).

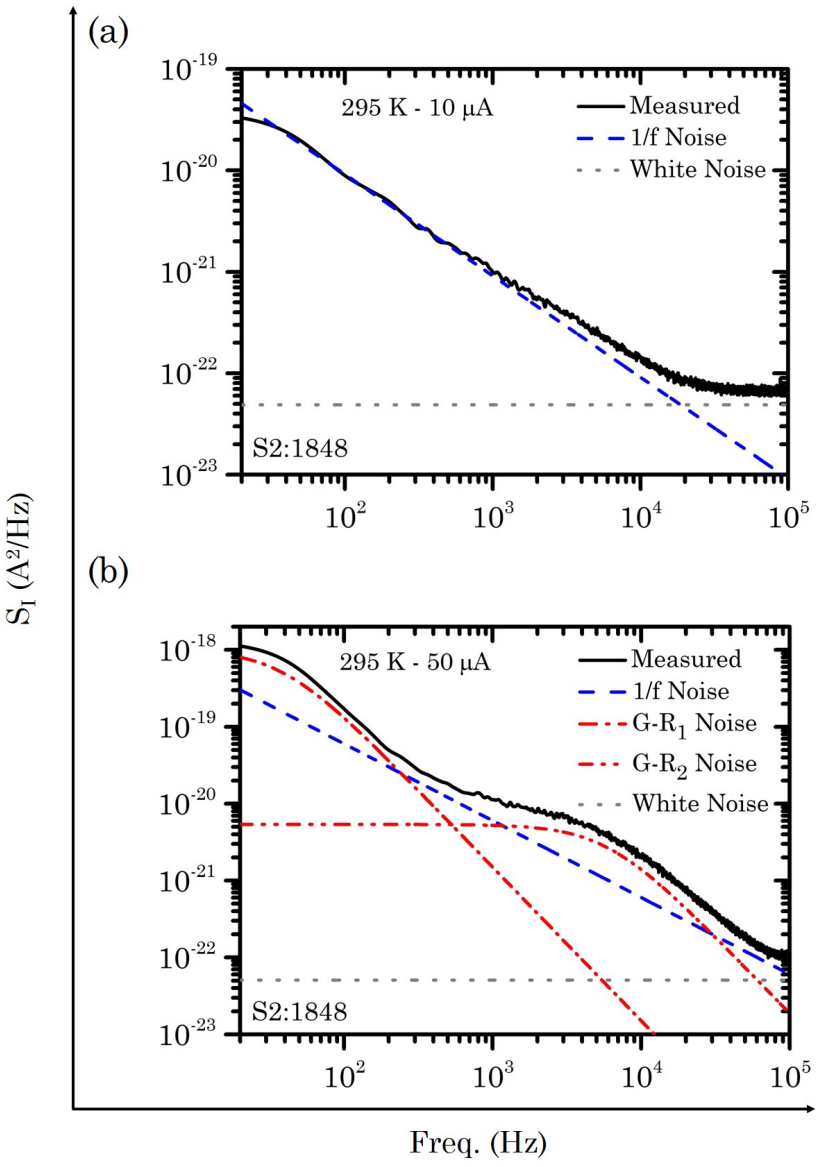

Figure 5.31: *The extracted components of the PSD spectra of the unannealed GaP/Si sample S2:1848, measured at room temperature with a bias current of (a) 10 μA and (b) 50 μA. Two different behaviours are seen: pure $1/f$ noise at the lower current and two $G-R$ noise peaks at the higher current.*

5.8.2 Trap Levels in the GaP/Si Heterostructure

It is interesting to speculate the existence of trap levels in the heterostructure film via investigation of the effect of temperature on the noise spectrum components. The PSD spectra of the samples S2:1848, measured at different temperature with flowing of a current of 100 μA, are shown in Fig. 5.32. Similar to what happened at the room-temperature measurements, the $G-R$ noise processes are clear, especially at a temperature of 180 K.

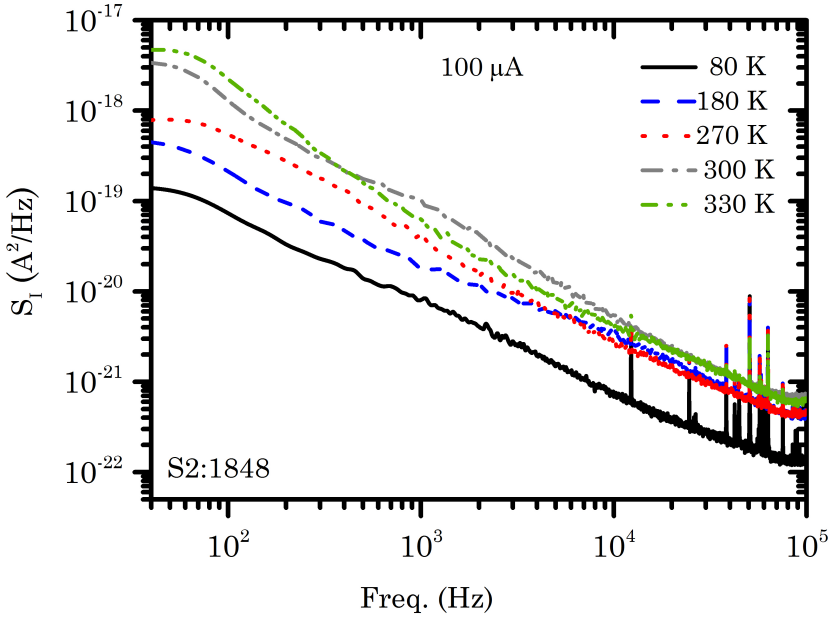

Figure 5.32: *Temperature-dependence PSD spectra of the unannealed GaP/Si sample S2:1848, measured at a bias current of 100 μA.*

The appearance of the Lorentzian peaks in the total noise spectrum confirms the formation of traps in the heterostructure [Ke-008]. An attractive method used to reveal the existence of trap level is the temperature-dependent normalized noise spectra. Figure 5.33(a) depicts such spectra for the sample S2:1848 measured at a bias current of 100 μA. These spectra have Lorentzian peaks appear at the corner frequency of the trap. The trap can be characterized by its time constant (τ_i), where $\tau_i = 1/2\pi f_i$.

By further examining the $G-R$ peak positions, shown in Fig. 5.33(a), we can see the increase of temperature gives rise to shift the peak towards higher corner frequencies. Thereby, by following these peaks, it would be able to get the Arrhenius plot for the dependence of the corner frequency on the temperature, as illustrated in Fig. 5.33(b).

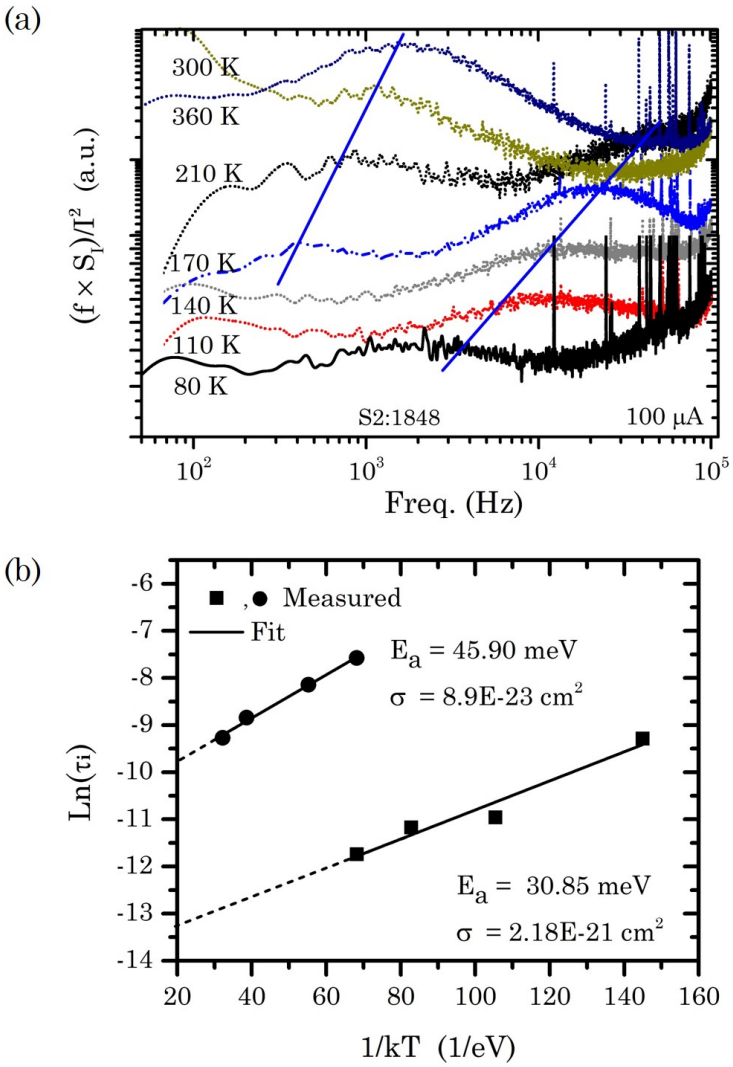

Figure 5.33: *(a) Temperature-dependent normalized PSD spectra of current noise of the unannealed GaP/Si sample S2:1848 for a bias current of 100 μA. (b) Arrhenius plot of temperature-dependent time constant of the traps.*

Practically, this plot is based on the trap time constant equation [Zie-86, Khl-05]:

$$\tau_i = \tau_\circ \exp\left(\frac{E_a}{kT}\right), \tag{5.21}$$

where $\tau_\circ$ is the atoms thermal vibration period, E_a is the thermal activation energy of trap and T is the temperature. The Arrhenius plot, depicted in Fig. 5.33(b), is thus obtained by plotting $Ln(\tau_i)$ against $1/kT$, which gives a line of slope equal to E_a. The intercept of the line with the y-axis gives the value of $\tau_\circ$, and consequently the capture-cross section of the trap (σ_t) can be calculated from ($\sigma_t = 1/\tau_\circ N_c V_{th}$) with N_c and V_{th} being the density of state of GaP and the electron thermal velocity.

N_c and V_{th} have the values of 1.8 $\times 10^{19} cm^{-3}$ and 2.73 $\times 10^{7} cm/sec$, respectively. Thus, two trap levels with E_a of 45.90 and 30.85 meV, and σ_t of 8.9 $\times 10^{-23}$ and 2.18 $\times 10^{-21}$ cm^2 are respectively identified.

5.8.3 LFN of the Annealed GaP/Si Heterostructures

A quite different behaviour of the noise measurements was observed in the annealed samples. Figure 5.34 confirms that the PSD plot of the sample S9:1902 is composed of $1/f$ and white noises only, while no $G-R$ peaks could be seen even though at a temperature of 80 K.

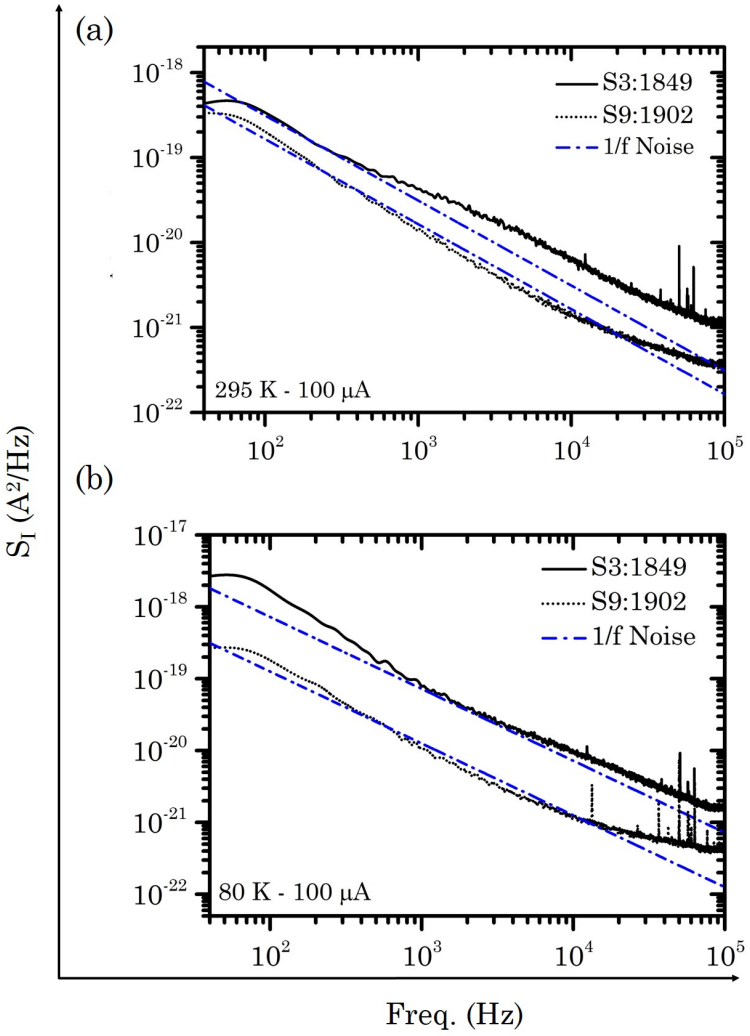

Figure 5.34: *A comparison between the PSD spectra of the unannealed GaP/Si sample S3:1849 and the annealed sample S9:1902 measured at room temperature and 80 K under a bias current of 100 μA.*

Likewise, under the influence of thermal annealing, the PSD spectrum of the annealed sample S6:1903, grown at 400 °C exhibited no $G-R$ noise component in comparison to the unannealed sample S2:1848. The noise spectra of this sample measured at room temperature by biasing the HJ diode with a forward current starts from 10 to 100 μA are illustrated in Fig. 5.35.

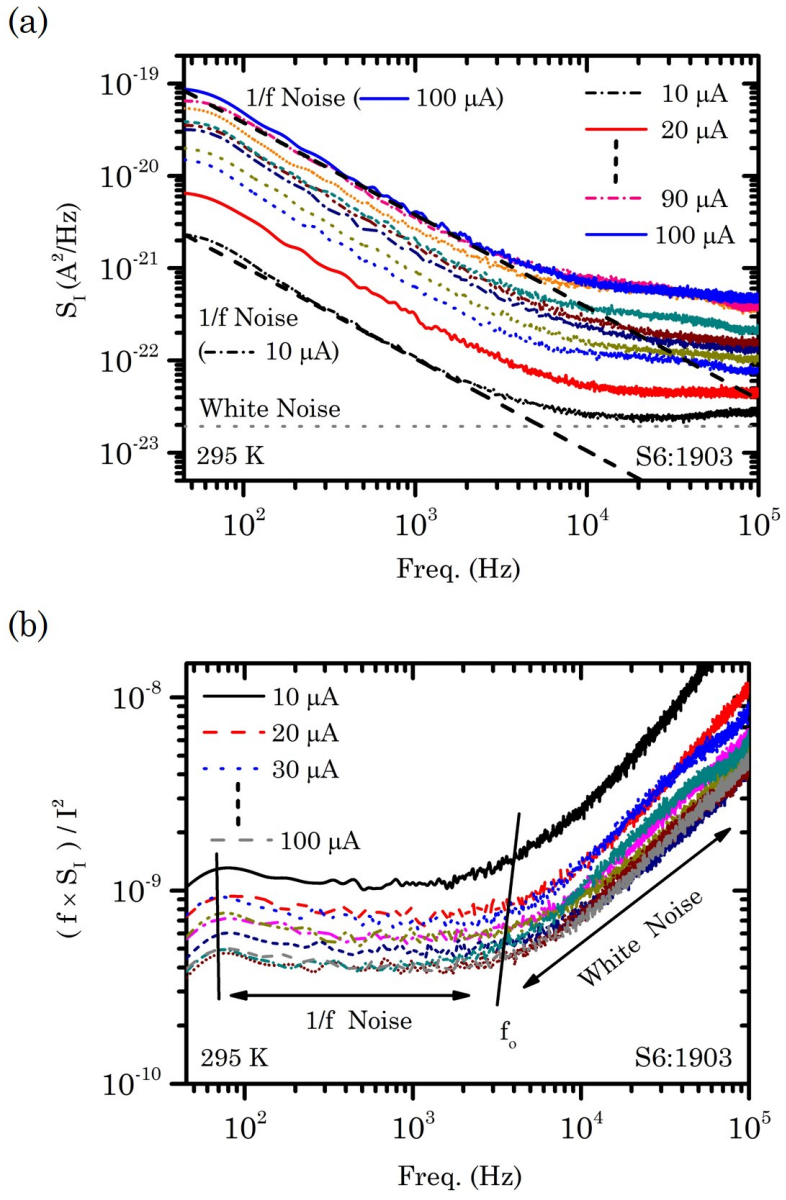

Figure 5.35: *Room-temperature PSD spectra of current noise of the annealed GaP/Si film S6:1903 for different bias current from 10 to 100 μA (a), and (b) their normalized PSD plots. No presence of $G-R$ noise processes.*

It seems pretty clear that all the spectra are $G-R$ noise free, and having pure $1/f$ in addition to the white noise components. Accordingly, the normalized spectra of Fig. 5.35(b) do not show any $G-R$ noise peak within the frequency range between 100 Hz and about 5 kHz. This case is also confirmed by the different-temperature noise measurements demonstrated in Fig. 5.36.

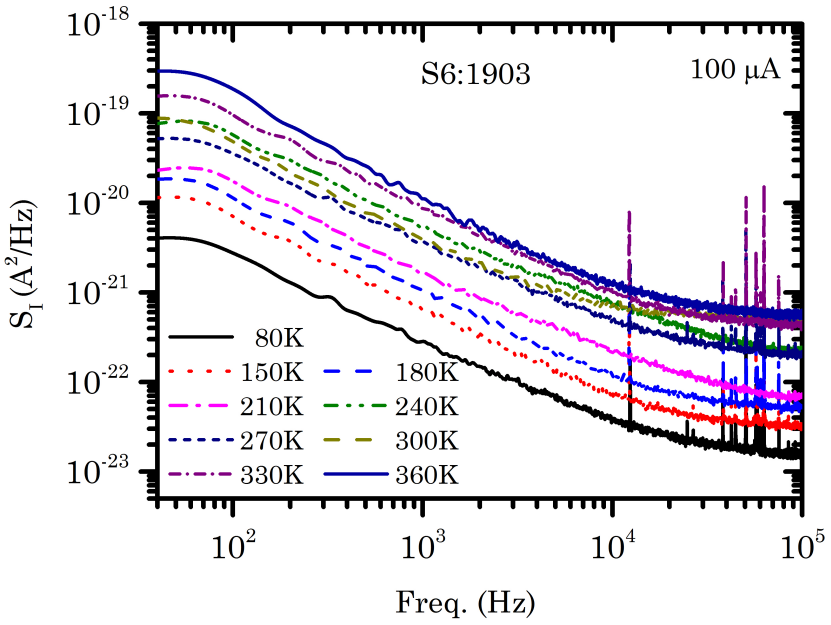

Figure 5.36: *Temperature-dependence PSD spectra of current noise of the annealed GaP/Si film S6:1903, measured at a bias current of 100 μA. All the spectra are free of $G-R$ noises.*

The remarkable finding in these measurements is that the noise level could be lowered by annealing. Due to annealing, the noise density level of the sample S6:1903 decreases respect to the unannealed film S2:1848 at all the bias currents. Figure 5.37 demonstrates an example for the room-temperature comparison between the PSD spectra of these samples at a current of 100 μA. Also, an identical case is observed in the noise spectra of the samples grown at 250 °C, as seen in Fig. 5.34.

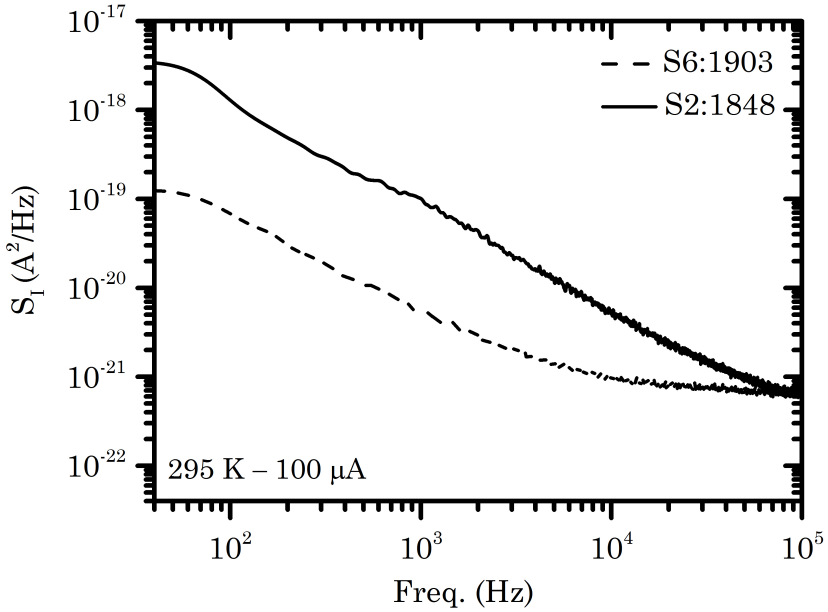

Figure 5.37: *A comparison of room-temperature current noise density of the GaP/Si films S2:1848 and S6:1903 for a bias current of 100 μA. The PSD level of sample S6:1903 is lowered due thermal annealing.*

5.8.4 Calculation of Hooge Parameter

In conformity with Eq. 2.20, the value of Hooge parameter is strongly dependent on the values of both $A_{1/f}$ and N. The later can be estimated depending on the charge carrier concentration (n) of the sample and its volume V, since $N = nV$. Such an estimation is easy for a layer whose dimensions are known. However, the situation in the diode, or even in the transistor, is somewhat different. This is because N of a $p-n$ junction is related to the depletion layer width, W, and the measured diode resistance, R_d. Therefore, R_d can be calculated by [Kuk-98, Kru-04, Lin-08, Pal-15]

$$R_d = \frac{W^2}{q\mu N}, \tag{5.22}$$

where μ is the carrier mobility. This equation can be expressed in terms of the junction conductivity and n as

$$R_d = \frac{nW^2}{\sigma N}. \tag{5.23}$$

Substituting Eq. 5.23 into Eq. 2.20 yields

$$\alpha_H = \frac{A_{1/f}}{R_d}\left(\frac{nW^2}{\sigma}\right). \tag{5.24}$$

When the bias current is changed from 10 to 100 μA, it is possible to extract different values of $A_{1/f}$ corresponding to different values of R_d. For example, the

variation of $A_{1/f}$ against R_d for the sample S6:1903 is demonstrated in Fig. 5.38. Thus, $A_{1/f}/R_d$ in Eq. 5.24 is obtained from the slope of this plot, and the other values; n, W and σ were already calculated from $C-V$ and $I-V$ measurements. It is believed that such method enables a more accurate estimation of α_H than using only one value of $A_{1/f}$.

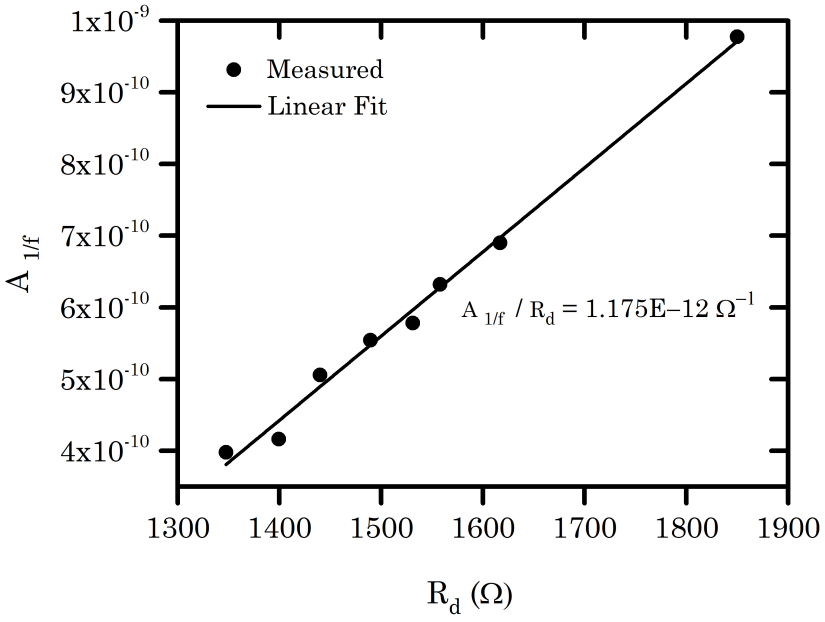

Figure 5.38: *Dependence of the flicker noise amplitude ($A_{1/f}$) on the diode resistance (R_d) of the GaP/Si sample S6:1903. $A_{1/f}$ values were extracted from LFN spectra under the bias current range from 10 to 100 μA.*

By using Eq. 5.24, the room-temperature α_H for some of the GaP/Si samples, estimated at the bias current range between 10 and 100 μA, are listed in Table 5.6.

Sample No.	T_g ($^\circ C$)	Annealing ($^\circ C/min$)	α_H
S2:1848	400	no	1.32×10^{-3}
S9:1902	250	(400-480)/90	7.41×10^{-4}
S6:1903	400	(400-480)/90	3.99×10^{-5}

Table 5.6: *Room-temperature Hooge parameters for the GaP/Si films S2:1848, S9:1902 and S6:1903 corresponding to a bias current range of 10 - 100 μA.*

It is noticed that a higher value of α_H corresponds to the bad-quality film, and the lowest value is correlated to the best-quality film, whereas the low-growth temperature annealed sample has in between value. Indeed, the difference among these values is an enough evidence that α_H is a measure of semiconductor quality.

5.8.5 Origin of Low-Frequency Noise

Regardless of the models presented to discuss the origin of LFN, it is often attributed to two prevailing theories: fluctuations of charge carrier mobility [Hoo-69] and fluctuations of free-charge carrier number [McW-57]. Anyway, the experiments can not accurately specify whether the measured noise absolutely matches the first or the second theory. In the obtained results, the relationship between S_I and the forward squared-bias current at frequency of 100 Hz, shown in Fig. 5.39, presents a quadratic dependence of S_I on the bias current.

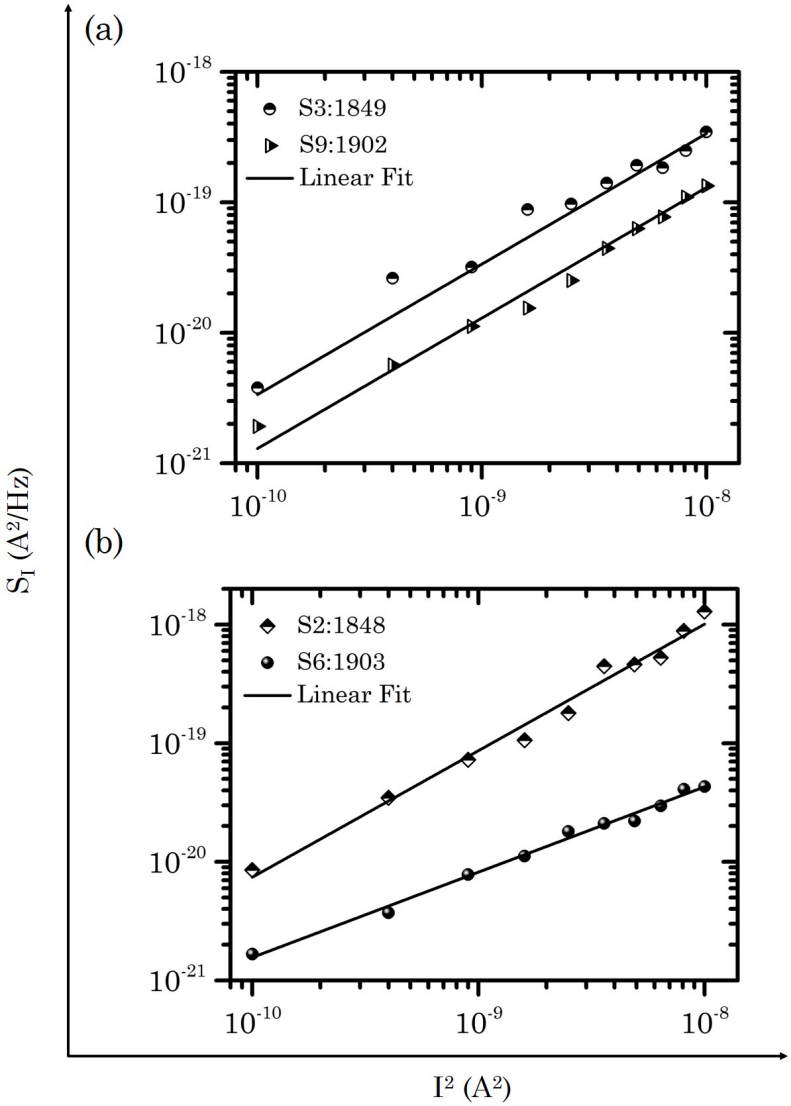

Figure 5.39: *Variation of S_I with the squared-bias current (I^2) at a frequency of 100 Hz for the GaP/Si samples (a) S3:1849 and S9:1902, and (b) S2:1848 and S6:1903.*

According to the Hooge formula ($S_I = C.I^2$, where $C = A_{1/f}/f$), the linear variation of S_I for all the samples with I^2 suggests that the 1/f noise origin obeys the Hooge model, and results from the junction resistance fluctuations [Kli-80, Aro-98].

To confirm this deduction, further checking of $S_I \propto I^2$ for these samples at different frequency values down to $f_\circ$ was tried. It was found that the linear variation was valid for the annealed samples, while a bit deviation from the linearity in the case of the unannealed samples was observed. This is attributed to the presentation of $G - R$ noise in the whole spectrum. Off course, such noise processes in the unannealed samples come from Δn, and hence the McWhorter model can also be satisfied [Sch-88, Sod-76]. As a result, both models are possibly applicable in the unannealed GaP/Si samples.

The disappearance of the $G - R$ processes in the noise spectra of the sample S6:1903 (Fig. 5.35) indicates that the traps generated in the unannealed sample was annihilated due to annealing. Such case possibly arises, when the traps are filled by electrons diffused in the layer during annealing. Besides that, as dislocations may act levels for trapping electrons, these levels can be exterminated by minimizing the dislocations by annealing. Thus, higher level of the noise spectrum of the sample S2:1848 in comparison to the sample S6:1903, illustrated in Fig. 5.37, could be brought about the increase of the $G - R$ noise level over flicker noise.

It is also observed that the level of $1/f$ noise of the samples S2:1848 (Fig. 5.32) and S6:1903 (Fig. 5.36) are much decreased at 80 K. This may be demonstrated in terms of free-charge carrier number. Since the carrier density is reduced at low temperature, the contribution of $G-R$ noise in the whole spectrum of the unannealed sample is expected to reduce because trapping or de-trapping electrons is decreased. It could also be attributed to the increase of resistance at low temperature, which might cause less fluctuation in the junction resistance.

5.9 Conclusion

Epitaxial GaP layers grown on Si substrates using GSMBE system were investigated. The layers were grown at substrate temperatures of 250, 400 and 550 °C with different thicknesses. Processing the layer in situ were performed by constant and step-graded thermal annealing with intoduction of PH_3 flux. The influence of the growth temperature, thermal annealing and layer thickness on the GaP layer quality were studied. Structural properties of the grown films were characterized using XRDs, SEM and AFM measurements. Then, the lattice shape was intensively analyzed by asymmetric XRDs and RSMs sketches. It was found that the lattice parameters of the GaP crystal are dependent of the above growth conditions, resulting in relaxed and compressive strained layers.

The growth conditions were optimized at a growth temperature of 400 °C with

a layer thickness of about 500 nm. At these conditions, the crystal quality of the epilayer annealed by step-graded method was highly improved, and the density of the dislocations in the system was reduced.

Moreover, transport properties of the heterostructures were studied using $I-V$ and $C-V$ characteristics. Some of the epilayers were found to be auto-doped, and rectification characteristics were obtained. The annealed films exhibited much reduction in the diode quality factors, confirming improvement in the crystal quality. Also, low-frequency $C-V$ characteristics confirmed that the depletion layer capacitance was strongly influenced by the frequency, due to more defects in the unannealed film in comparison to the annealed films. This is another evidence for reduction of defects by annealing.

Low-frequency noise measurements for epitaxial GaP/Si were intensively investigated. The components of the noise spectra were extracted and then the Hooge parameters for the heterostructure films were estimated. For GaP/Si HS, the Hooge parameter values were found to be in the order of 10^{-3} to 10^{-5}, which is decreased in the annealed film. The LFN results confirmed that the contribution of both $G-R$ noise and flicker noise in the total spectral density were reduced by thermal annealing. Additionally, it was found that the variation of the current passing through HJ gives rise to a linear variation in the 1/f noise level at a certain frequency. This behaviour is interpreted to obey the resistance fluctuations of Hooge model. Also, the $G-R$ processes presented in the LFN spectra are attributed to the fluctuations in charge carrier number model.

CHAPTER-6

Nanolithographic Patterns, Nanowires and Nanodiodes

Nanolithographic Patterns, Nanowires and Nanodiodes

Introduction

Electron-beam lithography is a versatile technique allows for creating an e-beam resist pattern on a substrate. The progress arising in this field has led to minimize microscale fabrications into sub nanometers applications. The main feature of the EB pattern is the possibility to form patterns with different shapes without using a mask as needed, for example, by photolithography. This chapter presents the procedure for fabrication of EBL patterns on the GaP substrates and the GaP/Si films. Thereafter, fabrication of GaP nanowires by MacEtch technique and characterization of the nanodiode array will be demonstrated.

6.1 Preparation of EBL Layer

The procedure for the fabrication of an EBL pattern consists of three steps: coating the substrate with an EB resist, printing the pattern and development of the pattern. The EBL process is usually followed by evaporation of metal on the printed pattern and lifting-off the unwanted metal. Before printing the pattern, the surface must be cleaned. N-type GaP (100) substrates and the GaP/Si (100) heterostructure films were chemically cleaned in isopropanol for 5 min in ultra-sonic system in order to remove particles attached to the surface, and then immersed in HF:H2O (1:100) for 30 sec to remove the oxide layer. For high resolution pattern, this step is necessary to avoid formation of defects in the resist, and to ensure well sticking the resist on the surface [Liu-02]. Immediately after cleaning the surface, it was baked on a hot plate at a temperature of 200 °C for 5 min to remove the residual water [Baj-05]. Then, the substrate was left to be cooled to room temperature.

Thereafter, PMMA resist of type 600 K, whose molecular weight is 600 kg/mol and a density of 0.97 gm/cm^3, was used for the EBL patterns. The resist layer was spun on the surface at a speed of 2000 and 6000 rpm for 45 sec producing thicknesses of about 310 and 180 nm, respectively, as measured by Alpha-Step 200 surface profiler. It was immediately baked on a hot plate at 160 °C for 3 min to improve the resist adhesion to the substrate [Dia-98]. Also, annealing the resist thermally leads to evaporate the solvents in the resist and helps to improve the surface roughness of the resist [Arj-09].

6.2 Systematic EBL Parameters

EBL patterns were printed on the PMMA resist using a JEOL JSM-6360 SEM connected to a Raith nanolithography system. The electron accelerating voltage was adjusted from 10 to 17 kV with an e-beam current between 0.006 and 0.01 nA. The image magnification can be adjusted from 200× to 1800×, which corresponds to bar scales of 200 μm and 10 μm, respectively. An EB column aperture of diameter of

2 μm is available in the SEM, and chosen for our work in order to direct a smaller spot size on the surface, which allows for nanoscale process. The blanker of the SEM system is controlled by Raith GmbH beam external electronic unit. Lithography process is computerized by an Elphy Plus software, which has a possibility for achieving different shapes of patterns. Matrices of 200 × 200 μm^2 and 40 × 40 μm^2 including patterns of circle mesh with diameters between 20 μm to 200 nm were printed on the PMMA resist. After printing the pattern, the sample was developed in a solution of (1:3) MIBK:IPA at about 10 °C for 50 sec, and then rinsed in IPA for 20 sec and blow-dried with N_2 gas.

6.3 Fabrication of Microscale Patterns

For simplicity, in order to approximately reach the optimal EB dose, the pattern was first designed in microscale and printed on a PMMA resist with a thickness about 310 nm. The systematic parameters were fixed to image magnification (Mag) of 450x, which corresponds to a bar scale of 100 μm, working distance, W_d, of 10 mm, beam spot size, S_p, of 50 nm, in addition to the accelerating voltage, V_{ac}, of 15 kV. Figure 6.1 shows a designed-pattern scheme of four squares of 100 × 100 μm^2. The dose for each square is equal to 100 $\mu C/cm^2$ times the factor (Fac), which is between 1 and 1.3.

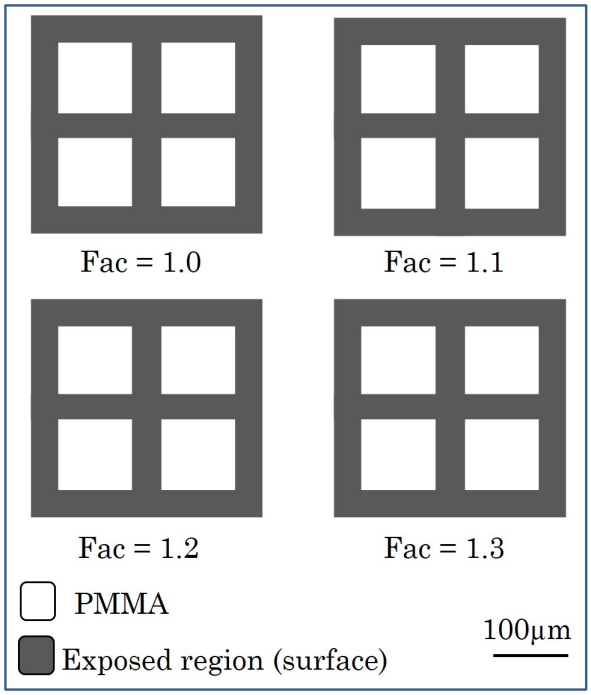

Figure 6.1: *A schematic representation for EBL designed pattern. The dimensions of small square is 100 × 100 μm^2.*

After developing the printed pattern, an Au layer of 50 nm was evaporated on the EBL pattern using a thermal evaporation system under a vacuum of 2×10^{-4} mbar. The evaporation rate was kept to 0.1 nm/sec, using a MIKI-FFV digital thin film monitor. Lifting-off the unwanted Au layer was carried out by dipping the sample in acetone for 60 min, producing the pattern shown in Fig. 6.2. It is seen that at a low EB dose (Fig. 6.2(a), the unwanted layer evaporated on the unexposed region is not lifted-off, while with increasing the dose, the layer is removed completely. Thus, for these pattern dimensions, the optimal dose is found to be 130 $\mu C/cm^2$ (Fig. 6.2(d)).

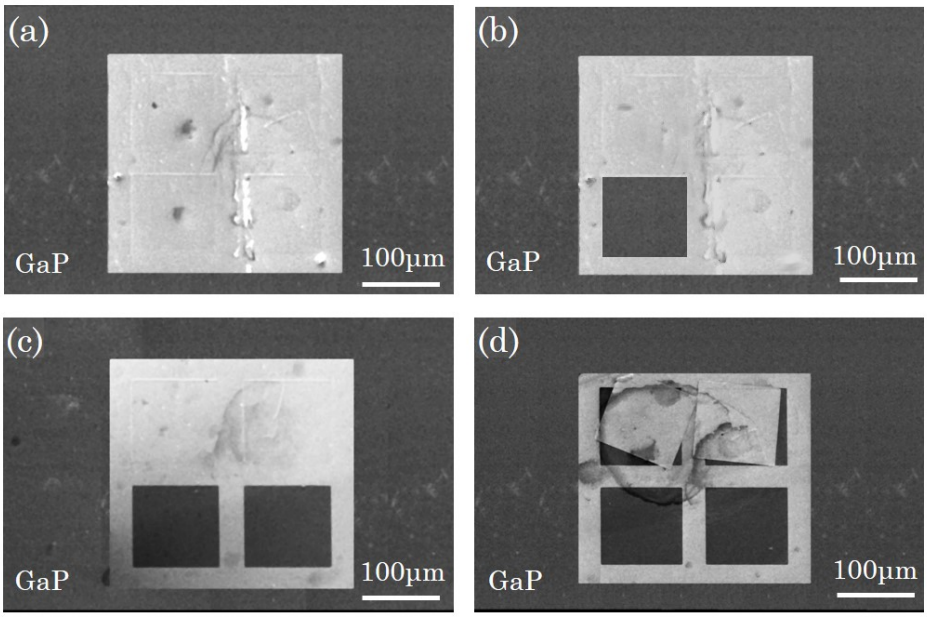

Figure 6.2: *SEM images of EBL pattern of Au layer on a GaP substrate. (a) Gold layer is not lifted-off, (b, c) Gold layers are partially lifted-off and (d) Gold layer is completely lifted-off.*

After this process, the pattern was designed such that it could consistent with our application, as shown in Fig. 6.3. In this pattern, the e-beam scans the regions around circles of diameter of 20 μm using an accelerating voltage of 15 kV. SEM images of the printed pattern after developing the PMMA resist is illustrated in Fig. 6.3(b, c). The beam dose was chosen to be changed from 110 to 165 $\mu C/cm^2$, where Fac $= 1 - 1.45$. Evidently, low doses are not sufficient to scan all the designed area. With increasing the dose to 143 $\mu C/cm^2$ (Fac $= 1.30$), the exposed region is completely removed after development.

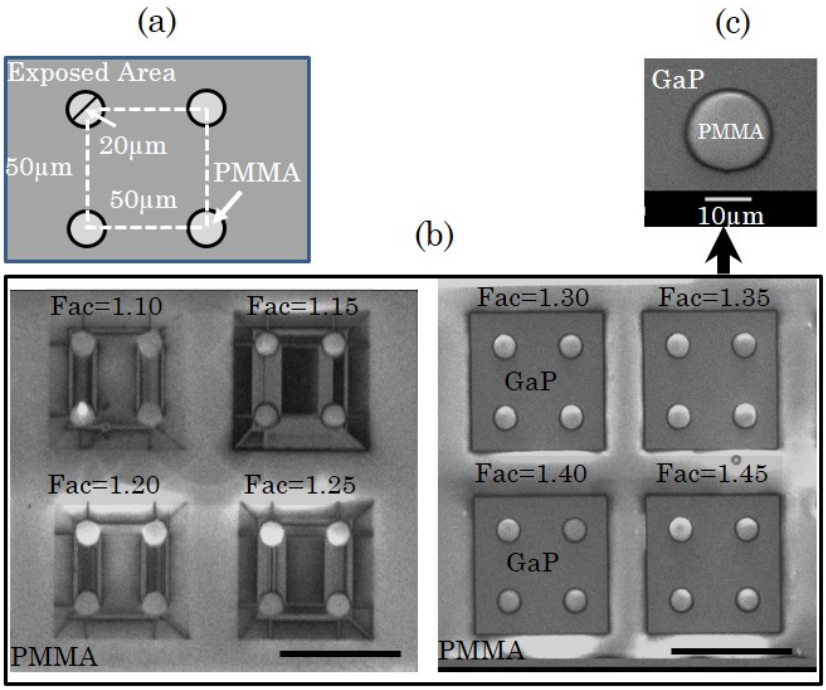

Figure 6.3: *(a) An EBL designed pattern of dots of 20 µm in diameter. (b) SEM image of the written pattern on a PMMA resist after development, with the bar scale of 100 µm. (c) Enlarged SEM image of the dot. The e-beam dose = 110 $\mu C/cm^2$ × Fac. The white regions in the images are due to space charge in the SEM.*

On the written pattern, an Au layer of thickness of 25 nm was evaporated, and then lifted-off by dipping the sample in acetone. Figure 6.4 shows SEM images of holes pattern of diameter of 20 μm.

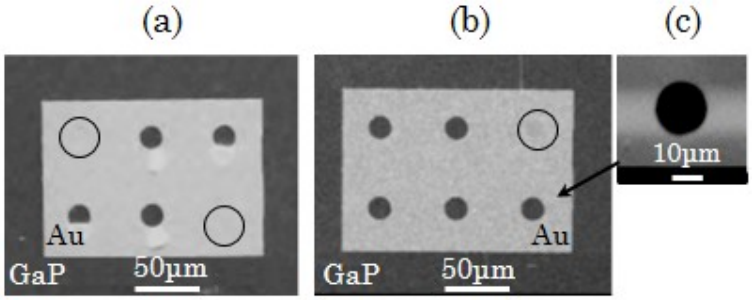

Figure 6.4: *SEM images of gold-hole pattern evaporated on an EBL pattern of dots of 20 µm in diameter written on the PMMA resist. The drawn circles represent the nonlifted-off holes. At the right hand, enlarged SEM image of the hole. The e-beam doses are equal to (a) 143 $\mu C/cm^2$ and (b) 165 $\mu C/cm^2$ (EB-Dose = 110 $\mu C/cm^2$ × Fac (1.3, 1.5)).*

Although the EBL pattern was well printed on the PMMA resist (Fig. 6.3), lifted-off metal failed in some exposed regions, because some of the holes were closed with the Au layer. This result suggests that a V-type edge was mostly occurred in the exposed area leading to stick the gold on the wall of the resist. That means, the dose was low, so the pattern was then perfectly inverted to the Au layer by applying higher doses ranging between 170 - 180 $\mu C/cm^2$, as shown in Fig. 6.5.

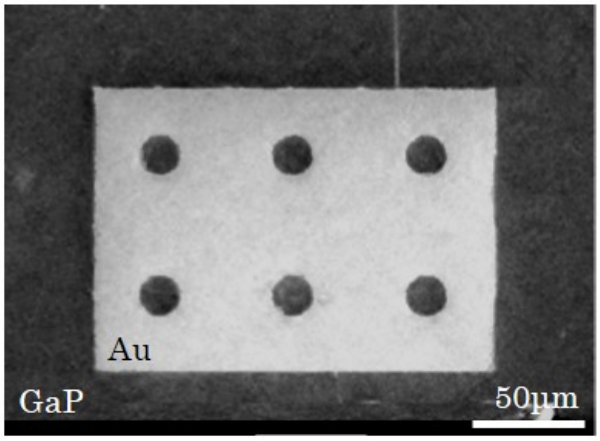

Figure 6.5: *SEM image of gold pattern evaporated a GaP substrate with holes of 20 μm in diameter. E-beam doses ranging between 170 and 180 $\mu C/cm^2$.*

Thus, this magnitude of the e-beam dose was firstly adopted for smaller-feature pattern. Figure 6.6 shows an Au pattern of holes with diameter of 5 μm printed on a GaP substrate with a dose of 170 $\mu C/cm^2$.

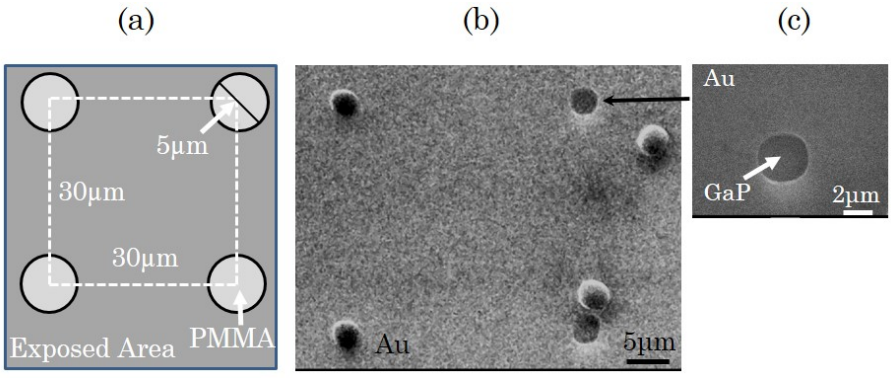

Figure 6.6: *(a) Design of dot pattern of 5 μm in diameter. SEM image of Au pattern evaporated on the EBL pattern written on the PMMA resist. E-beam dose = 170 $\mu C/cm^2$. (c) Enlarged SEM image of the hole.*

6.4 Accelerating Voltage Factor

The energy of incident electrons has an effective role for determining the resolution of the pattern, due to the interaction of electrons with the resist. To study the pattern resolution dependence on the accelerating voltage, the diameters of the holes were then decreased to 300 nm. Shown in Fig. 6.7 is a simulation for the interaction of an e-beam at different accelerating voltage: (a): 12 kV, (b): 15 kV and (c): 17 kV, with PMMA of thickness of 310 nm using Casino software version 2.4. It is seen that higher voltage results in deeper penetration of the e-beam into the substrate with more divergence (Fig. 6.7(c)).

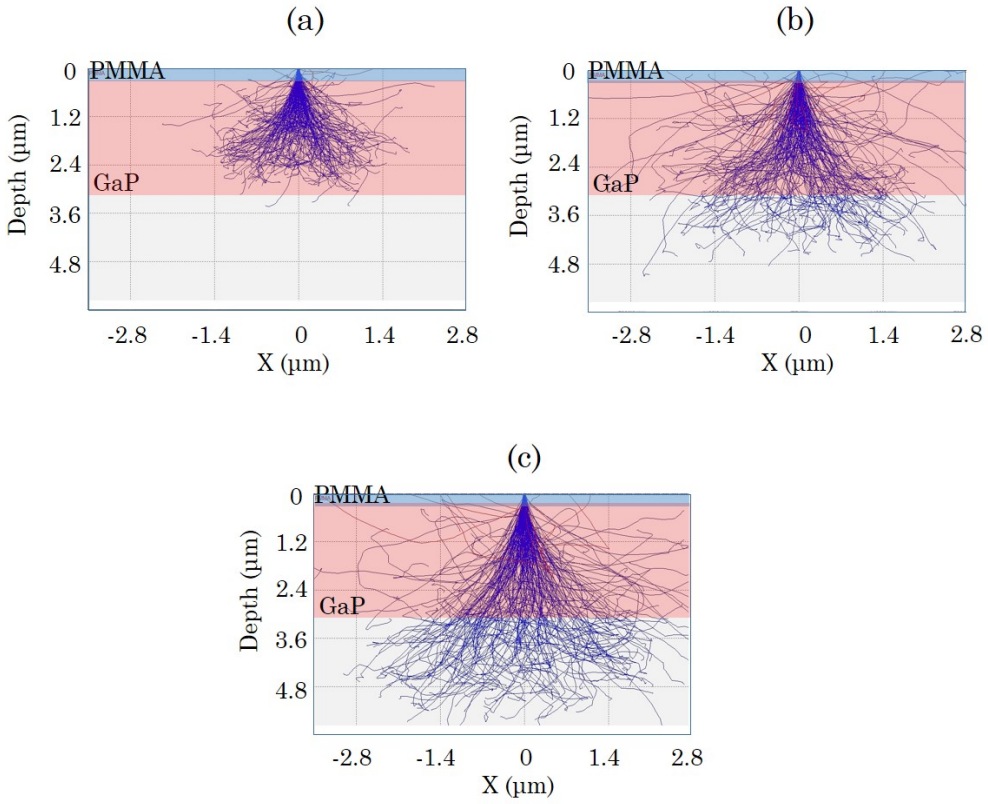

Figure 6.7: *Casino simulation of the interaction of an e-beam at an accelerating voltage of (a) 12, (b) 15 and (c) 17 kV with PMMA of 310 nm in thickness on a GaP substrate. Divergence of the beam in the substrate increases with the voltage.*

Figure 6.8 shows developed patterns at V_{ac} of 12, 15 and 17 kV and exposed by an e-beam dose of 120 $\mu C/cm^2$. No clear pattern was obtained at the voltages lower than 12 kV, because the electrons haven't enough energies for penetrating into the substrate. At voltages of 15 and 17 kV, some of the holes are not opened (inside the white circles). This action can be interpreted in relation of interaction of elec-

trons with the resist. At higher voltage, the electrons can gain higher energies, and when they interact with the PMMA resist, many fragments would be produced at the exposed region [Moh-11]. During development process the fragments could be stiffened on the edges leading to close some holes. Therefore, at 15 kV pattern, the number of the closed holes is reduced. The resolution of the holes is thus better at an accelerating voltage of 12 kV.

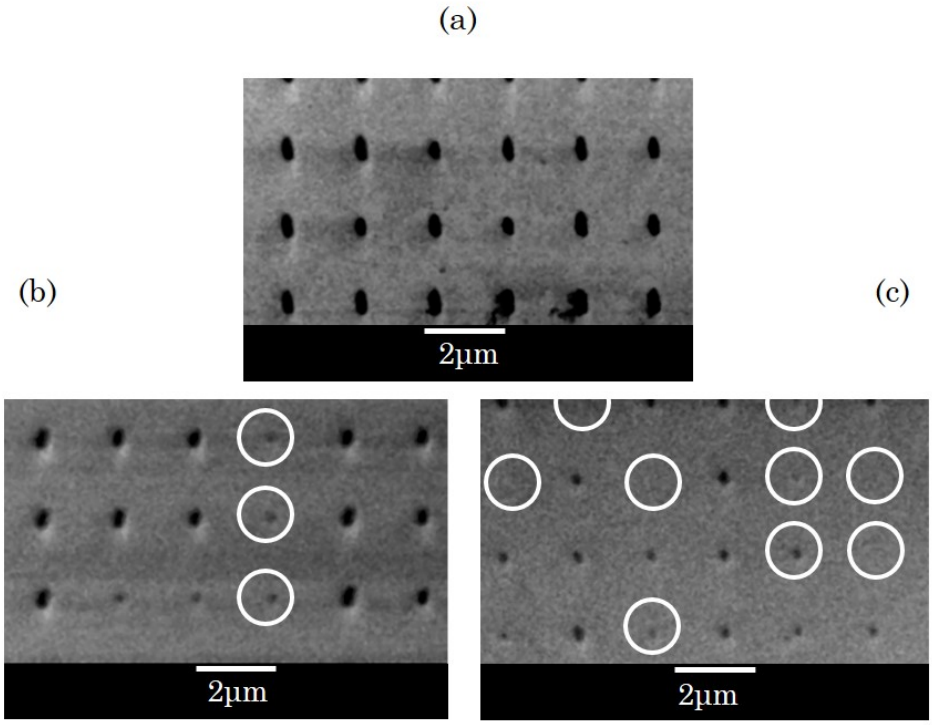

Figure 6.8: *SEM images of holes pattern of 200 nm in diameter written on a PMMA resist after development using an accelerating voltage of (a) 12 kV, (b) 15 kV and (c) 17 kV, and an EB dose of 120 $\mu C/cm^2$. The circles show the distorted holes.*

6.5 Correction of EB Astigmatism

When astigmatism of the lenses is not adjusted, the e-beam spot becomes not fully circular, making the shape of the written pattern slightly different from the designed pattern. A clear example for such effect is demonstrated in Fig. 6.9. Here, the printed shape is oval, since the astigmatism increases in the vertical direction. Hence, the astigmatism must be gently corrected in order to avoid any distortion in the pattern.

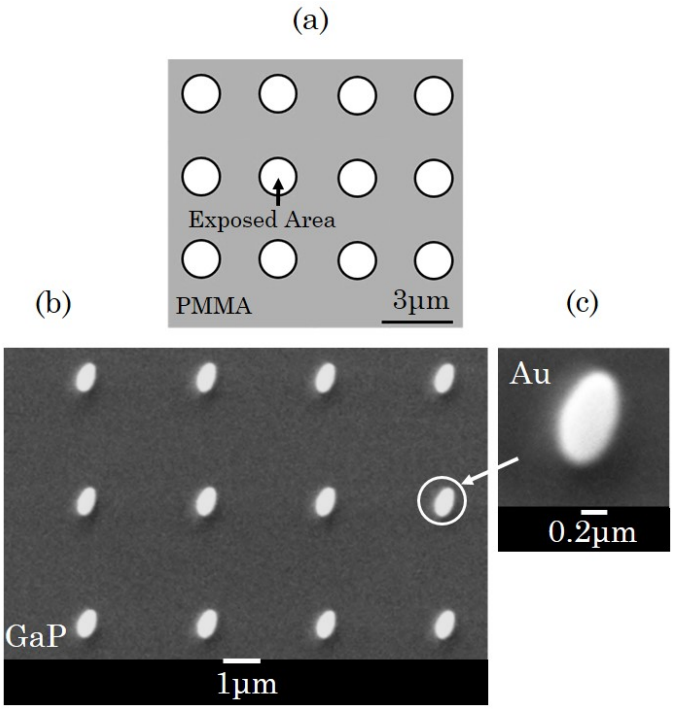

Figure 6.9: *A comparison between the designed hole pattern (a) and the printed pattern on a GaP substrate (b). Although the designed pattern is circular, an oval-shape pattern is seen (c). The distortion in the hole shape is caused by presenting the astigmatism in the e-beam.*

6.6 Optimization of Lift-off Process

The written pattern can be transferred from the PMMA resist to a metal layer by implementing lift-off process. As soon as this process has been ended, the obtained pattern may reveal whether the optimal lithographic conditions are satisfied or not. In other words, the metal pattern rejects a negative image for the pattern. Then, the quality of the resulting structure is assessed by the SEM images.

This process was performed by immersing the sample in acetone for different times. Figure 6.10 shows lift-off process of Au layer on a GaP substrate with holes of diameter of 20 μm (Fig. 6.10(a, b, c)), and on GaP/Si films with holes of diameter of 600 nm (Fig. 6.10(d, e, f)). It was found that dipping the sample in the acetone for 30 min (Fig. 6.10(a, d)) and 60 min (Fig. 6.10(b and e)) led to partially lift-off the gold from the surface. Therefore, as the acetone does not impact on the pattern shape, the time required for this process was increased more than three hours in order to give the acetone a sufficient time to penetrate into all holes. This case is confirmed in Fig. 6.10(c, f).

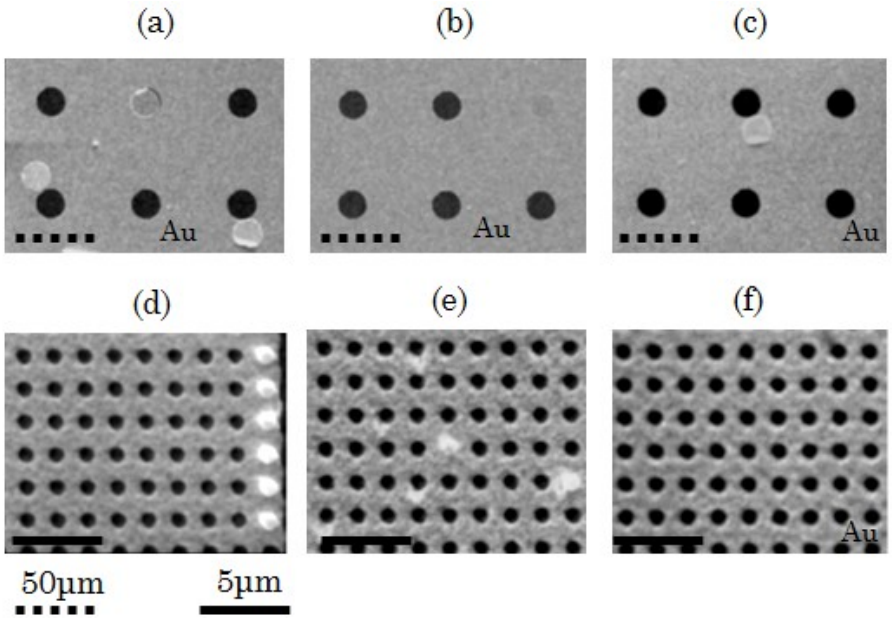

Figure 6.10: *Lift-off process of the gold layer from a GaP substrate (a, b, c) and GaP/Si films (d, e, f). The layer is partially lifted-off after immersing the film in acetone for 30 min (a, d) and 60 min (b, e), while it is completely lifted-off after a long time in acetone (c and f).*

6.7 Fabrication of Nanoscale Pattern

It is well-established that a 12 kV is the optimal accelerating voltage for nanoscale-feature pattern. In Fig. 6.6, we have seen that the dose required for printing 5 μm hole pattern is 170 $\mu C/cm^2$. The magnitude of the EB dose must be reduced for smaller-feature pattern, otherwise the edge of the hole will be slightly exposed, and finally the hole diameter is reduced. Accordingly, starting from holes of diameter of 3 μm, 2 μm and so forth, the dose magnitude was chosen to start from 150 $\mu C/cm^2$.

Moreover, this figure shows that lifting-off Au was not performed completely. Therefore, it was necessary to change some of the beam-scanning conditions. The beam spot-size must be minimized and the magnification of the SEM image must be maximized. Therefore, S_p was decreased to 25 nm, while smaller than this value was not possible, since it leads to a very blur image. Also, Mag was maximized to 1800×, by which the maximum working area became 40 × 40 μm^2.

Another significant parameter is the resist thickness. The dot size of the printed pattern, shown in Fig. 6.11, does not fully match the designed pattern, since the diameters of the designed and the printed patterns are 200 nm and 235 nm, respectively, using an EB dose range between 130 and 140 $\mu C/cm^2$. One possible reason behind that is the divergence of the e-beam increases with the resist thickness, ac-

cording to Eq. 3.1. Therefore, to minimized such effect at a given accelerating voltage, the thickness is decreased to 180 nm. This finally led to match the designed pattern to the printed one, and improve the lift-off process.

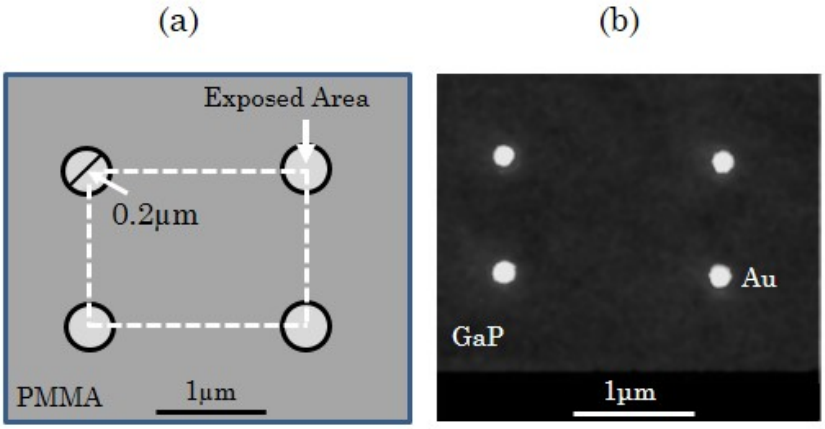

Figure 6.11: *(a) Designed pattern of holes of diameter of 200 nm. (b) Gold-dot pattern of diameter about 235 nm evaporated on the EBL pattern of PMMA resist printed on a GaP substrate. E-beam dose = 135 $\mu C/cm^2$.*

The above lithography conditions were used for hole patterns and resulted in perfect patterns. Figure 6.12 shows Au patterns for holes of diameters of 3 μm and 2 μm printed on GaP substrates using an e-beam dose of (a) 150 $\mu C/cm^2$ and (b) 130 $\mu C/cm^2$.

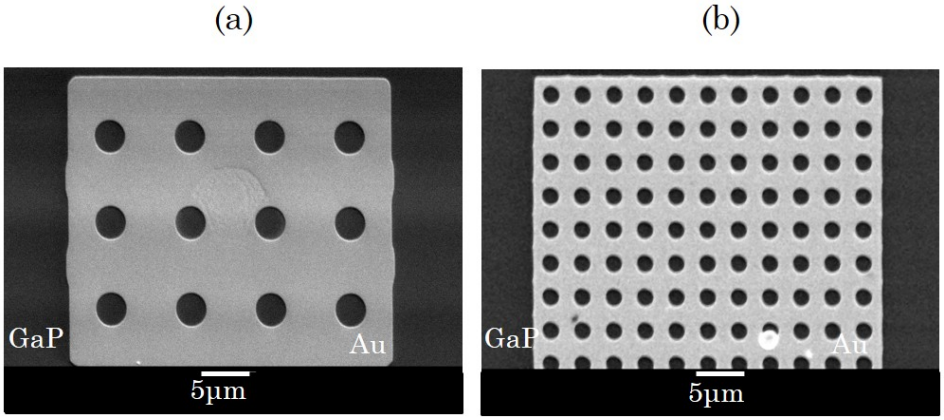

Figure 6.12: *SEM images of gold-hole patterns evaporated on EBL patterns of PMMA resist printed on GaP substrates. The holes diameters and the e-beam doses are (a) 3 μm and 150 $\mu C/cm^2$, and (b) 2 μm and 130 $\mu C/cm^2$, respectively.*

Obviously, perfect lift-off process, and holes of highly-contrast edges are seen in this figure, as well as it was found the printed pattern was perfectly matching the

designed pattern.

When the hole feature is decreased to nanoscale, it becomes hard to recognize the edges and the shape of the hole. Therefore, it is desirable to use dot pattern, which allows checking the contrast of the edges by SEM. After optimizing the dot pattern, we could convert it to hole pattern, bearing in mind the need to a bit change in the dose magnitude. An optimized nanoscale pattern of Au dots is shown in Fig. 6.13. In these patterns the dots exhibit highly contrast with a perfect lift-off process.

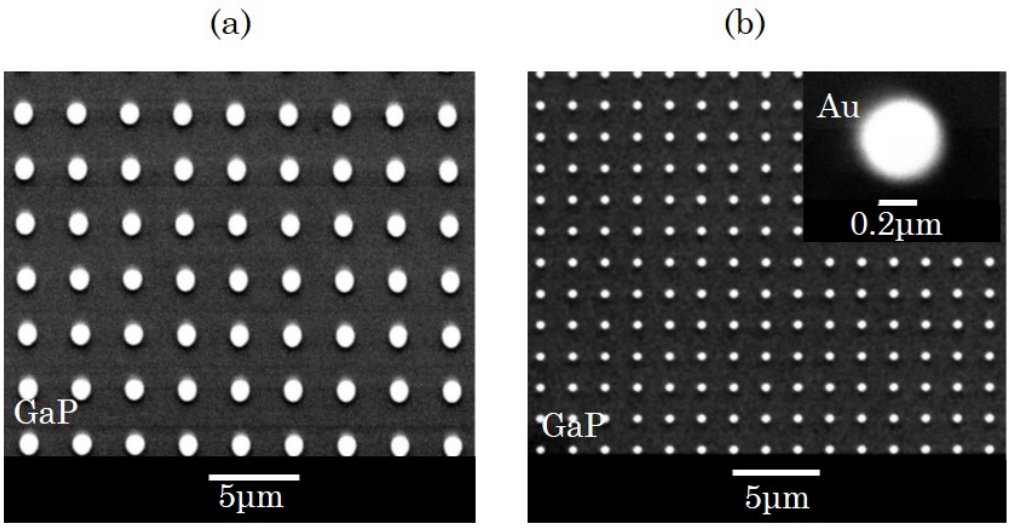

Figure 6.13: *Gold-dot patterns evaporated on EBL patterns of PMMA resist printed on GaP substrates. The dot diameters and the e-beam doses are (a) 900 nm and 150 $\mu C/cm^2$, and (b) 300 nm and 135 $\mu C/cm^2$, respectively.*

Since the nanoscale-dot pattern was optimized at the same above parameters, they were adopted for the hole pattern except the dose was changed. Figure. 6.14 shows two Au nanopatterns of holes with diameters about 600 nm and 200 nm converted to GaP substrates. These patterns were optimized at doses between (a) 115 - 135 and (b) 80 - 95 $\mu C/cm^2$.

The EB dose is dependent on the exposed area (A) according to below equation:

$$Dose = \frac{I_B\ t}{A}, \tag{6.1}$$

where I_B is the EB current and t is the exposure time. In all the experiments, the value of I_B was approximately kept between 6 - 10 pA. This equation tells us that when the exposed area increases, the EB dose must be reduced, provided that the values of I_B and t are kept constants. Accordingly, if the diameter of the unexposed region is required to be as small as possible, the exposed area should be increased, and consequently the EB dose should be reduced.

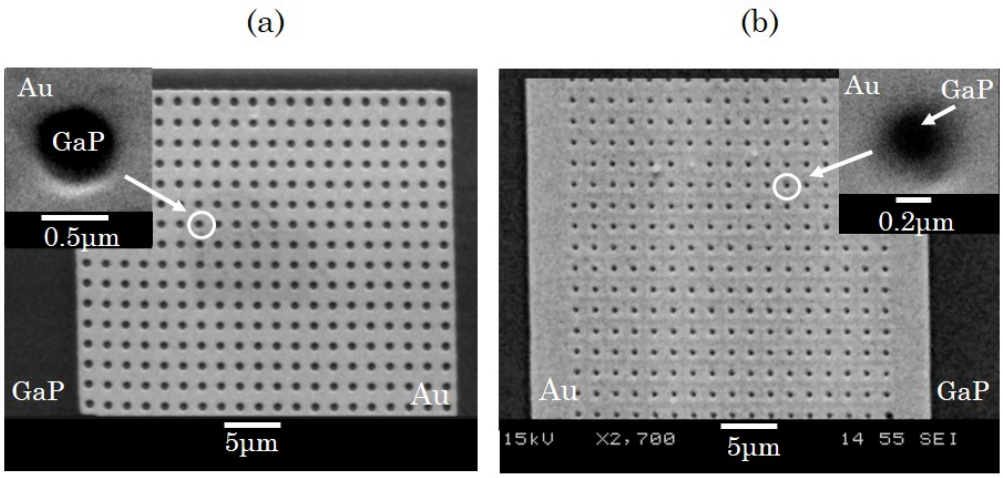

Figure 6.14: *Gold-hole patterns of about 600 nm and 200 nm in diameters with an e-beam dose of (a) 115 and (b) 90 $\mu C/cm^2$ evaporated on GaP substrates.*

From the above results, it is possible to plot the dependence of the hole feature on the EB dose under V_{ac} of 12 kV, as shown in Fig. 6.15. This clearly shows that lower EB dose is required for printing smaller-diameter holes.

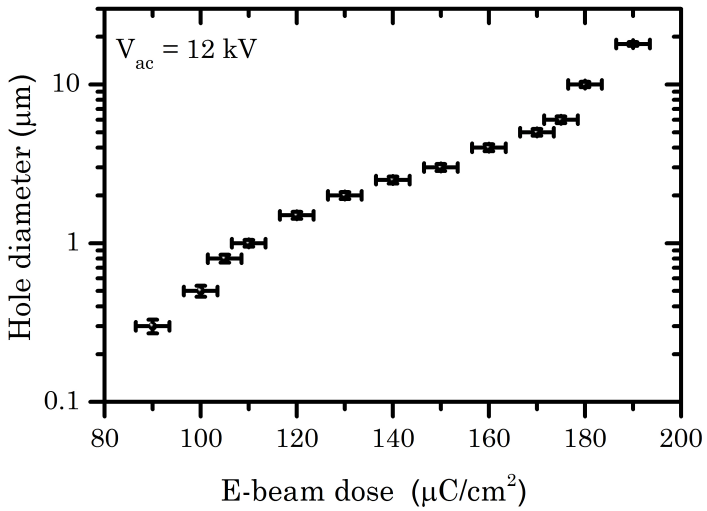

Figure 6.15: *The dependence of the hole diameter on the e-beam dose at V_{ac} of 12 kV. For smaller feature, lower EB dose is required.*

The EB nanopattern described above was carried out on GaP substrates, because the surface is very smooth. Therefore, since the surface of the GaP/Si heterostructure is rougher than the GaP substrates, it was reasonably expected that at least the EB dose should be changed. Applying the same conditions on the GaP/Si film (S4:1893), for example, the Au pattern was not lifted-off, as shown in Fig. 6.16,

even though the dose range was extended to 140 $\mu C/cm^2$. The hole diameter of the designed pattern was chosen to be 2 μm, whereas the metal pattern showed non-lifted holes of diameters about 1.6 μm.

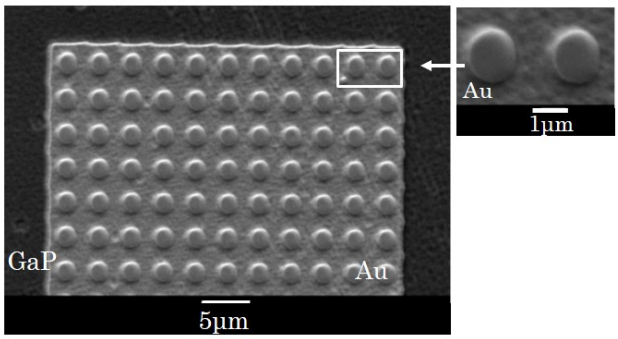

Figure 6.16: *A gold-hole pattern of 2 µm in diameter converted to a GaP/Si sample S4:1893 using an e-beam dose of 133 $\mu C/cm^2$. The film shows a bad lift-off process.*

This finding suggests that either a V-type printing shape occurred or the resist thickness is small so that the metal on the exposed area could adhere to the unexposed one. This problem was solved by slightly increasing the thickness to about 190 nm. Then, as illustrated in Fig. 6.17, a good hole pattern with diameters about 200 nm and density about 1.5 $\times 10^8$ cm^{-2} was obtained.

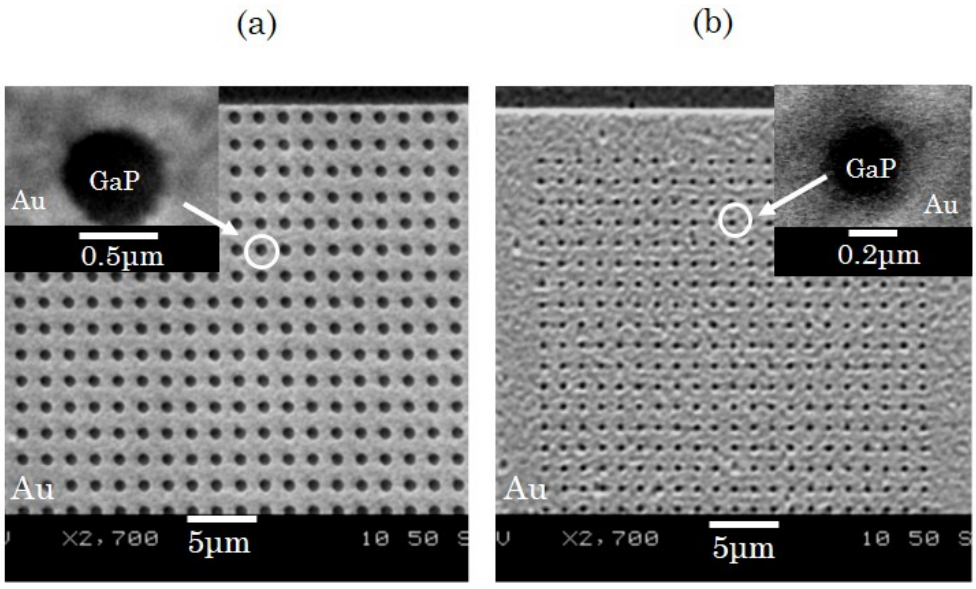

Figure 6.17: *Gold-hole patterns converted to the GaP/Si sample S4:1893. The hole diameters and the e-beam doses are about (a) 600 nm and 133 $\mu C/cm^2$, and (b) 200 nm and 90 $\mu C/cm^2$.*

6.8 Metal-Assisted Chemical Etching of GaP

MacEtch is a directional wet etching technique catalyzed by a thin layer of a noble metal occurs in the semiconductor region underneath the metal, while the surrounding region should not be influenced by the etchant solution. Limited kinds of solutions are currently used for MacEtch of III-V compounds: a mixture of $KMnO_4$ and H_2SO_4 for etching GaAs substrate [DeJ-11], and a mixture of H_2O_2 and HF for etching GaP nanocones [Kim-16]. However, in the presented work, various solutions at different temperatures were tried. The concentrations of the chemicals used in MacEtch as well as calculations of the solution molarities are demonstrated in Appendix A.2. In addition to the GaP epilayers, n-type GaP substrates of doping concentration of 10^{16} cm^{-3}, patterned with Au layers of thickness of 25 nm, were used for the MacEtch experiments.

The GaP substrates were firstly etched in a mixture of H_2O_2:HF, whose molarities are 28 and 11.9 mol/Lit, respectively. Figure 6.18 shows the effect of oxidant concentration on the vertical-etching rate (E_V) of the GaP substrate with different concentrations of HF. The magnitude of E_V increases as the etchant concentration increases.

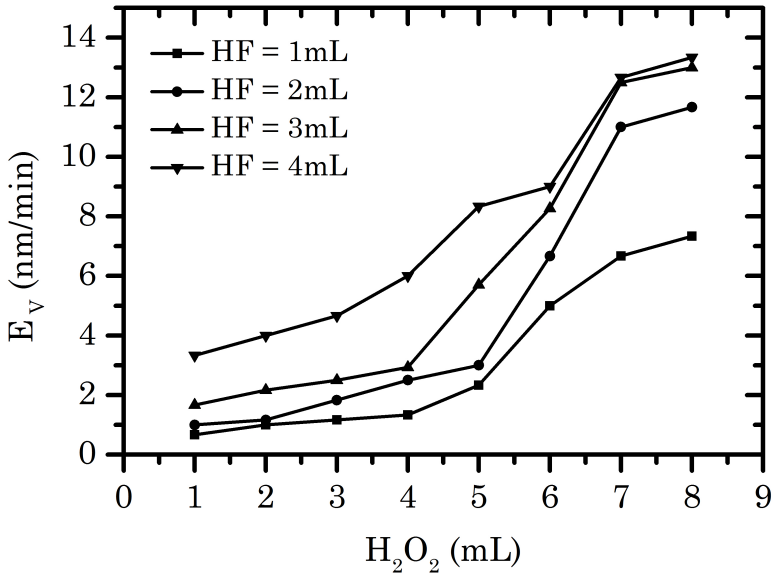

Figure 6.18: *Vertical-etching rate of the GaP substrate as a function of H_2O_2 concentration with different concentrations of HF for 30 min.*

These measurements were carried out using a 50 × 50 μm^2 Au-square pattern at room temperature during 30 min. But, it was observed that the Au layer started to lift-off from the substrate after 10 min of etching, using a solution of (5 mL)H_2O_2:(8 mL)HF:(10 mL)H_2O. As shown in Fig. 6.19(a), most of the metal pattern is removed

under these concentrations, leaving a low etched region underneath about 500 nm. Moreover, using this mixture with different concentrations to etch the GaP epilayer led to collapse the layer, as shown in Fig. 6.19(b).

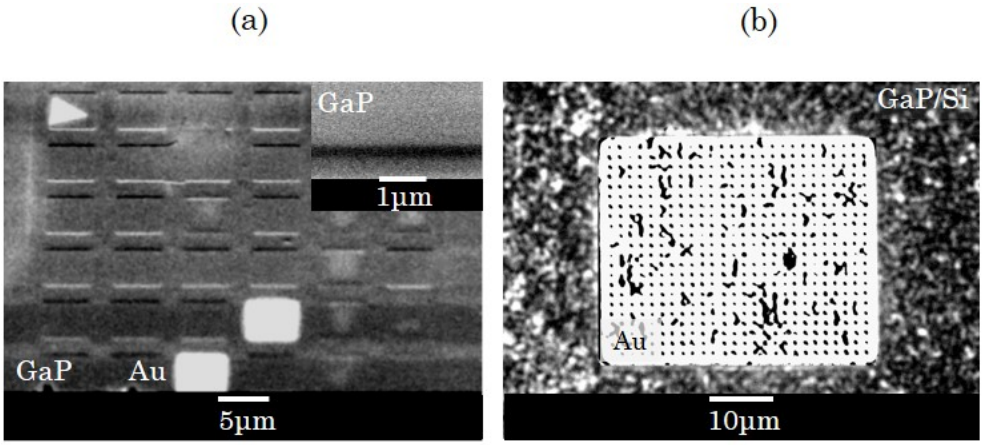

Figure 6.19: *(a) Front-view SEM image of room-temperature MacEtch of 50 × 50 μm^2 gold-square patterned GaP substrate using a mixture of (5mL)H_2O_2:(8mL)HF:(10mL)H_2O for 30 min. (b) High-resolution image for MacEtch of the GaP epilayer using the same concentrations.*

In keeping with these results, the use of H_2O_2 as an oxidant is not useful for our structure. This may be attributed to the strong chemical potential of H_2O_2 (1.77 V), which could lead to etch the region around the metal strongly. Instead, a weaker potential oxidant, such as $KMnO_4$ with a chemical potential of 1.51 V, is thought to prevent etching of non-metallic region, and maintain etching underneath metal [DeJ-11]. Hence, $KMnO_4$ together with H_2SO_4 were used as etchant solution. The SEM images of MacEtch of the GaP substrate and the GaP/Si epilayer at temperatures between 40 and 50 °C using a mixture of (3 mL)$KMnO_4$:(2 mL)H_2SO_4:(20 mL)H_2O for 10 min are shown in Fig. 6.20. In this case, the vertical etching is increased in comparison to what occurred by using H_2O_2.

Alternatively, it was observed that when the feature size is decreased to sub microns, the Au layer was lifted-off after a few minutes of etching, and the epilayer became rough, as shown in Fig. 6.20(d). Therefore, sticking of an Au-mesh pattern of 40 × 40 μm^2 on the surface was not maintained long time in such solution.

It should be noted that the room-temperature etching was very low in spite of using different concentrations. Thus, as Au is quickly lifted-off and the surface becomes rougher, it is most likely that H_2SO_4 has a strong effect, leading to etch the surface and reduce the vertical etching as well. Hence, according to this interpretation, it was necessary to replace H_2SO_4 with another acid. Unfortunately, most of strong acids such as nitric acid (HNO_3), HCl and hydrobromic acid (HBr), were

experienced and they gave either similar results or no etching. On the other hand, weak acids, e.g. acetic acid (CH_3COOH), did not result in vertical etch. Finally, HF was chosen instead of H_2SO_4.

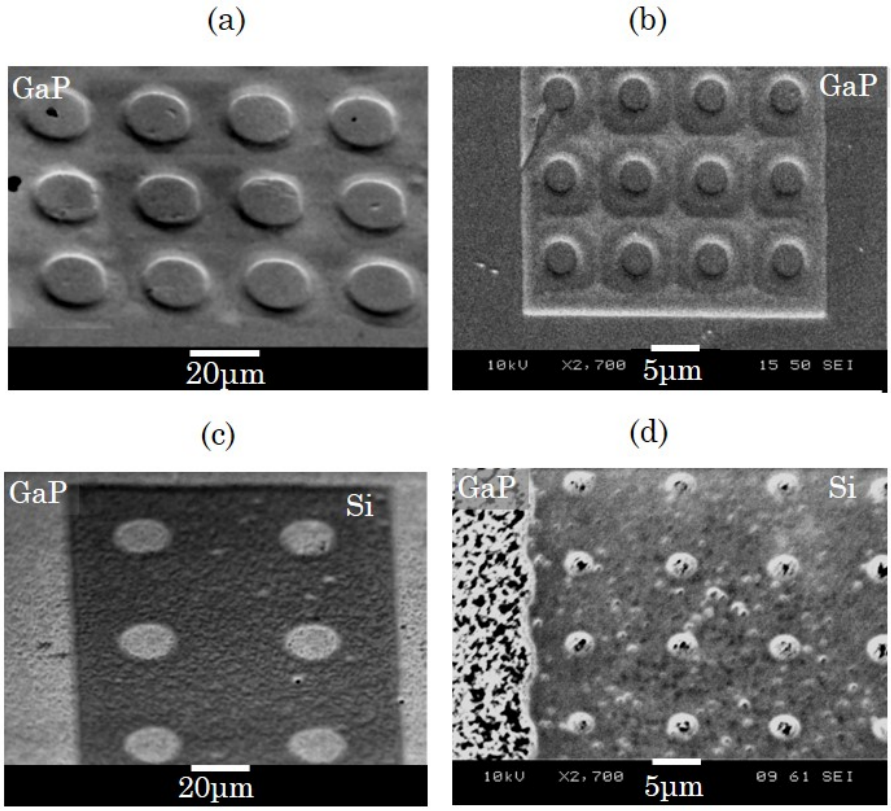

Figure 6.20: *SEM images of MacEtch of GaP substrate (a and b) and GaP epilayer (c and d) using gold mesh of diameters of 20 and 5 µm, respectively. MacEtch was carried out using a solution of (3 mL)$KMnO_4$:(2 mL)H_2SO_4:(20 mL)H_2O for 10 min at 40-50 °C.*

6.8.1 MacEtch of GaP at Room Temperature

The GaP substrate was first etched by a solution of (100 mM)$KMnO_4$:(1 M) HF with volumes of 2 mL and 3 mL, respectively. A cross-sectional SEM image of room-temperature etching of GaP, using a 100 × 100 μm^2 gold stripe, for 20 min is shown in Fig. 6.21(a). In this figure, the etching ratio (E_t) of E_V to the side etching rate (E_H) is calculated to be about 1.26. The same process was carried out using a gold-hole pattern of diameters of 10 μm, as shown in Fig. 6.21(b). Large side etching is seen in both images.

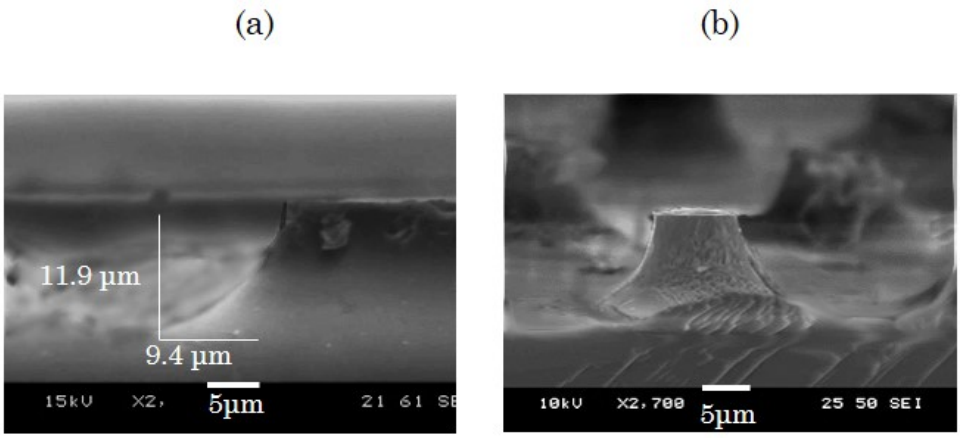

Figure 6.21: *Cross-sectional SEM images of MacEtch of GaP in a mixture of $KMnO_4$:HF of molarity of 100 mM and 1 M for 20 min, respectively, catalyzed by (a) a gold strip of area of 100 × 100 μm^2, and (b) a gold pattern of holes of diameters of 10 μm.*

Since E_H was so large, the concentration of the oxidant was reduced to 25 mM, resulting in an E_t of 5.4, where E_H was reduced, as illustrated in Fig. 6.22(a). Similarly, as shown in Fig. 6.22(b), the hole pattern produces a larger etching rate compared to that shown in Fig. 6.21(b). That means, the reduction of oxidant concentration can maintain the vertical etching and weaken the side etching.

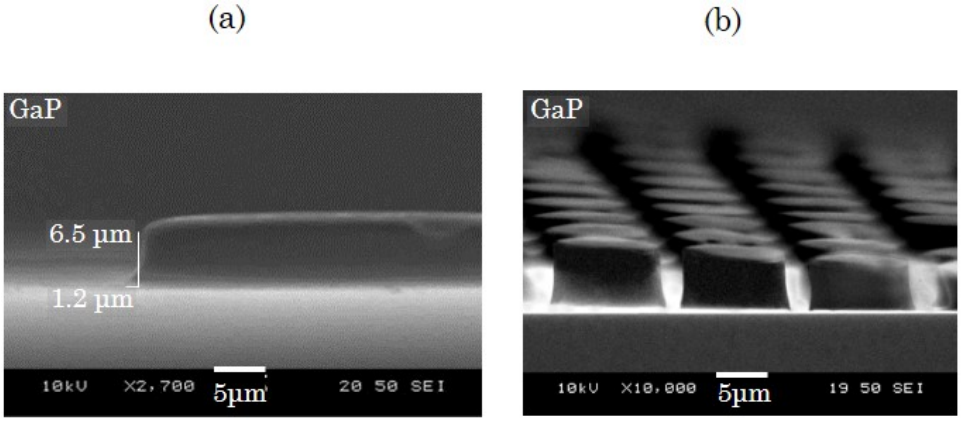

Figure 6.22: *Cross-sectional SEM images of MacEtch of GaP in a mixture of $KMnO_4$:HF of molarity of (a) 25 mM catalyzed by a gold strip of an area of 100 × 100 μm^2 for 20 min, and (b) 1 M catalyzed by a gold mesh with hole diameter of 10 μm.*

The dependence of the MacEtch process in GaP substrate on the $KMnO_4$ concentration using 1 M of HF is plotted in Fig. 6.23. All the measurements were carried out by mixing 2 mL of $KMnO_4$ of various concentrations with 3 mL of HF. Clearly,

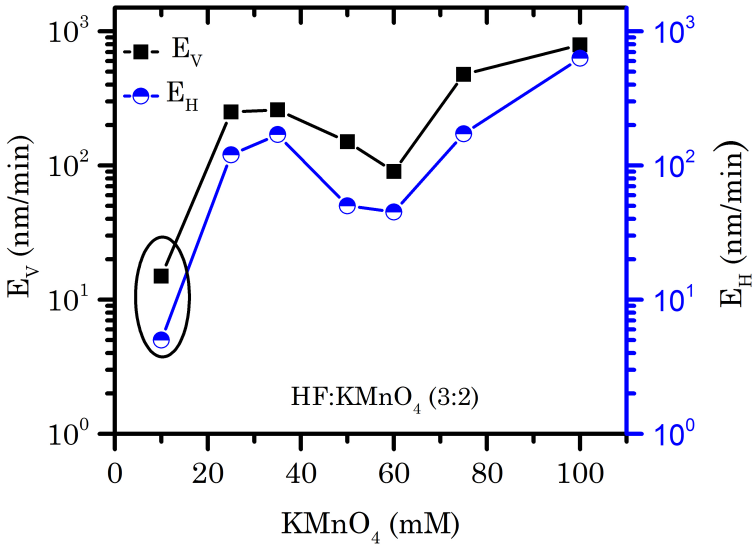

Figure 6.23: *MacEtch of the GaP substrate as a function of $KMnO_4$ concentration with 1 M of HF. The difference between E_V and E_H has a maximum value at $KMnO_4$ concentration of 10 mM.*

the maximum ratio of E_V/E_H is obtained at a concentration of 10 mM of $KMnO_4$.

Using the same solution concentrations; (2 mL)$KMnO_4$:(3 mL)HF, for the MacEtch of GaP substrate, catalyzed by a 20 × 20 μm^2 Au mesh of holes with a nominal diameter of 1.2 μm, is shown in Fig. 6.24. The value of E_V measured in this figure is about 70 nm/min, which confirms that 10 mM is the best value could be adopted for the next etching process.

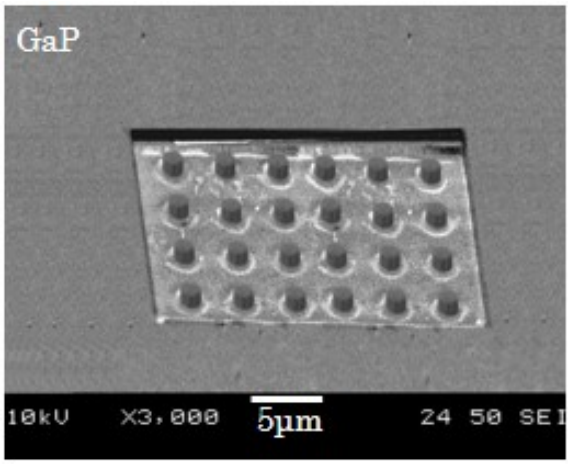

Figure 6.24: *SEM image of the MacEtch of the GaP substrate using solution of (2 mL)$KMnO_4$:(3 mL)HF with E_V about 70 nm/min, catalyzed by a 20 × 20 μm^2 gold mesh with hole diameters of 1.2 μm.*

Further experiments to reach the optimal volume ratio (R_V) were carried out, where $R_V = V_{HF}/V_{KMnO_4}$. These solution concentrations, (10 mM) $KMnO_4$ and (1 M) HF, were taking into consideration, while the volume ratio was changed. For example, mixing of 10 mL from 1 M-HF with 10 mL from 10 mM-$KMnO_4$ leads to $R_V = 1$. A comparison of MacEtch process in a GaP substrate under different volume ratios is illustrated in Fig. 6.25. When the ratio is around 2, the maximum difference between the vertical and side etching can be obtained.

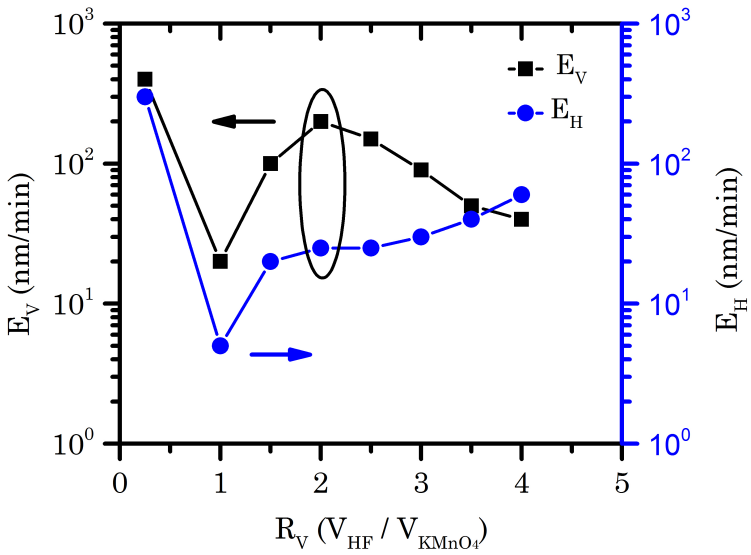

Figure 6.25: *MacEtch of GaP as a function of HF/$KMnO_4$ volume ratio (R_V) catalyzed by a gold mesh. The maximum difference between the vertical and side etching appears at a ratio around 2.*

6.8.2 Inverse MacEtch of GaP

An opposite action was observed, when the concentration of $KMnO_4$ exceeded 125 mM and heating the solution to 60 °C. By such conditions, it is most likely the oxidant attacks GaP strongly, whereas the Au-layer behaves as a mask can protect the region underneath. Thereby, an inverse MacEtch would be occurred. Figure 6.26 shows a microscale structure produced by the inverse MacEtch of GaP substrate at 60 °C using (125 mM)$KMnO_4$:(1 M)HF, and catalyzed by arrays of Au dots with diameters of 5 and 2 μm as masks.

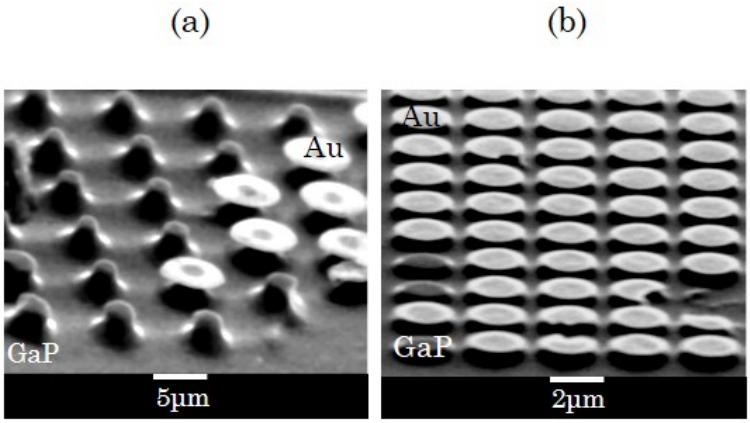

Figure 6.26: *Inverse MacEtch in GaP substrate produced by gold-dot array at a temperature of 60 °C using concentrations of (125 mM)$KMnO_4$:(1 M)HF.*

6.8.3 MacEtch of GaP at High Temperature

Since the optimal room-temperature ratio of $HF/KMnO_4$ was determined to approximately 2, MacEtch process at higher temperature was also experienced. The GaP substrates and the GaP epilayers were etched at a temperature range of 35−50 °C, using the same above ratio. At temperatures less than 40 °C, there was no much difference in the etching than that obtained at room temperature. Alternately, at the temperature range between 40 and 45 °C, E_V was enhanced with lower E_H. GaP NWs of diameters about 700 nm fabricated by MacEtch of the GaP substrate and the GaP epilayer for 15 min at this temperature range catalyzed by Au-layer meshes are shown in Fig. 6.27.

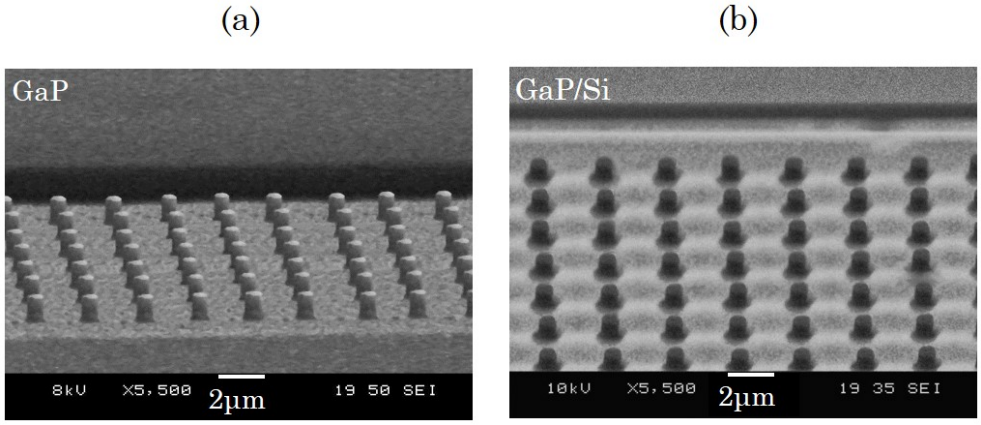

Figure 6.27: *SEM images of nanowires fabricated by MacEtch process in the GaP substrate and the GaP epilayer catalyzed by a gold-mesh of hole diameters about 700 nm.*

It is remarked that at temperature of 50 °C, the Au layer was quickly lifted-off causing bad etching, because the side etching was enhanced. As demonstrated in Fig. 6.28, the structures resulted from high-temperature etching is distorted as a result of decreasing vertical etching. In other words, at high temperature, the etching underneath the metal becomes rough causing lifting-off the metal and thereby the solution will attack the epilayer completely, which enhances the side etching.

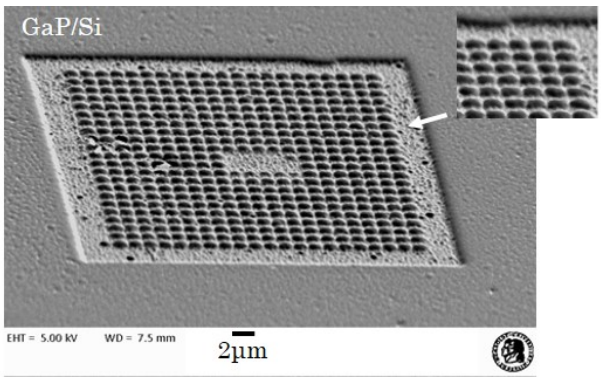

Figure 6.28: *SEM images of MacEtch process in the GaP epilayer catalyzed by gold mesh of holes of nominal diameters about 900 nm at a temperature of 50 °C.*

Applying the above etching conditions using smaller feature hole patterns, smaller diameters nanowires were then fabricated. Figure 6.29 illustrates GaP NWs of nominal diameter of 200 nm, and density between 1 and 3 $\times$ 10^8 cm^{-2}, fabricated using MacEtch process in the GaP substrate for 25 min and the GaP epilayer for 10 min catalyzed by Au layer meshes.

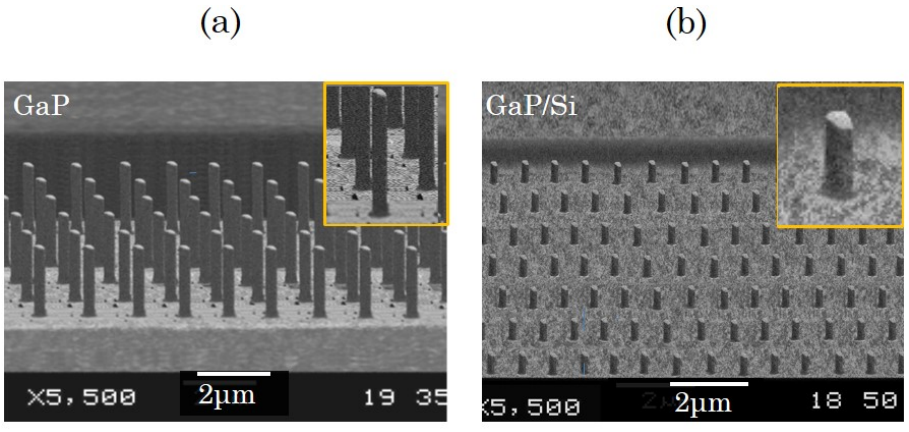

Figure 6.29: *SEM images of nanowires of nominal diameter of 200 nm fabricated by MacEtch process in the GaP substrate and the GaP epilayer catalyzed by gold meshes using HF/$KMnO_4$ solution.*

6.9 Nanodiode Array Fabrication

Since the GaP/Si heterostructures exhibited diode characteristics, the nanostructures produced by the MacEtch process were thereby employed for the fabrication of nanodiode array. Figure 6.30 demonstrates the steps used for the device fabrication.

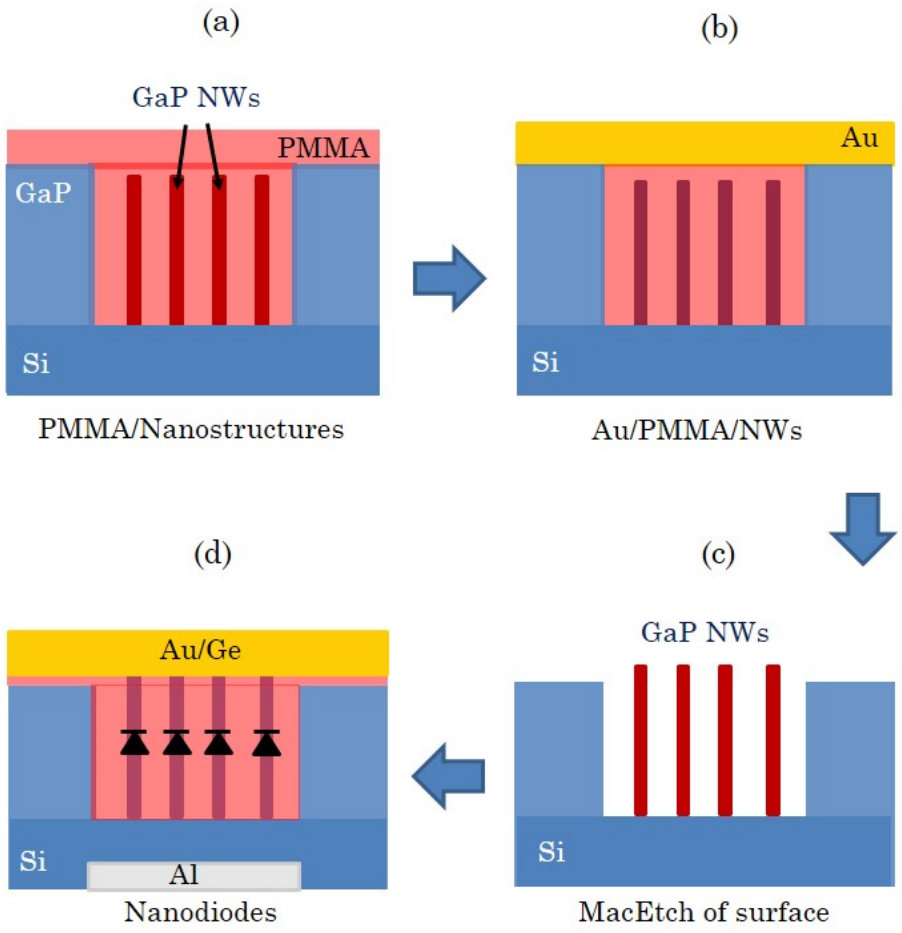

Figure 6.30: *The sequence of steps required for the nanodiodes fabrication. (a) Spinning of PMMA resist on the structure and surface, (b) a thin gold layer is evaporated on the surface, (c) MacEtch of the region around the structure, (d) spinning of PMMA resist on the structure and surface followed by evaporation of Ohmic contacts; Au/Ge for the cathode and Al for the anode.*

A PMMA resist was first spun on the surface covering both the nanostructures and the surrounding non-etched region (Fig. 6.30(a)). The resist was then developed many times, without using lithography process, in order to decrease its thickness gradually. After few minutes of development, the resist was removed from the surface, whereas the nanostructures were still covered by the resist. Thereafter, a 25

nm Au-layer was evaporated on the surface in order to perform the MacEtch process for the region around the structure (Fig. 6.30(b, c)). This operation led to decrease the height of the layer surface, and finally the nanowires became higher than the surface. Again, PMMA resist was spun and developed, followed by evaporation of a thin layer of Au/Ge as a cathode contact. The resist can isolate the semiconductor around the nanostructure from the contacts. An Al layer was then evaporated on the Si back side to be used as a contact for the anode (Fig. 6.30(d)). Finally, the sample was dipped in acetone to lift-off the unwanted metallic layer on the resist.

6.9.1 Fabrication of Ohmic Contacts

Two types of Ohmic contacts were fabricated on the backside of Si and on the top of GaP NWs. Prior to evaporation of contact, the Si backside was chemically cleaned by dipping the sample in the solutions described in Sec. 5.1.1 for four minutes, without using US system to avoid the damages might arise in the nanostructures. Before this process, the contact resistance was determined using photolithographic pattern. The pattern was printed on ma-N 440 negative-tone photoresist spun on the surface at speed of 3000 rpm for 30 sec, and then baked at 95 °C for 5 min. These spin conditions provide a resist film with thickness of 4.1 μm [Mic-09]. After printing the pattern, the sample was developed in a ma-D322s solvent for 60 sec, and then stopped by DI for 10 sec and blow-dried with N2 gas.

Al is commonly used for Ohmic contacts on Si due to good adhesion, low resistivity and suitable for Si solar cell [Nor-71, Mei-98, Raj-09]. For these aspects, Al was suggested as an ohmic contact to the Si substrate. To avoid penetrating Al spikes into Si substrate, a 5 nm of Ni layer was evaporated to form a barrier between Si and Al. Then, an Al-layer of thickness of 100 nm was evaporated on Ni with an evaporation rate of 0.1 nm/sec.

The Ohmic contact to GaP was already studied by different groups using Au, Ag, Al and Ni [Nak-71], and using Au/Ni and Au-Ge/Ni [Mal-85, Pet-03]. From their results it was concluded that minimum-resistivity Ohmic contacts can be obtained by forming Au-Ge/Ni contacts on GaP. Anyway, in this work, a 5 nm of Ni layer was evaporated on the GaP surface, followed by evaporation of an Au-Ge (88:12 wt%) layer with thickness of 100 nm. After that, the metal was lifted-off by dipping the sample in acetone for 5 minutes. Then, the contacts were annealed in N_2/H_2 gas for 60 sec at a temperature of 400 °C.

Figure 6.31 illustrates the metallic contact pads on the Si substrate and on the GaP layer. Six contact pads having equal areas (A) of 100 × 400 μm^2, and separations $D_1, D_2 ... D_5$ of 20, 40, 100,200 and 400 μm, respectively, were made.

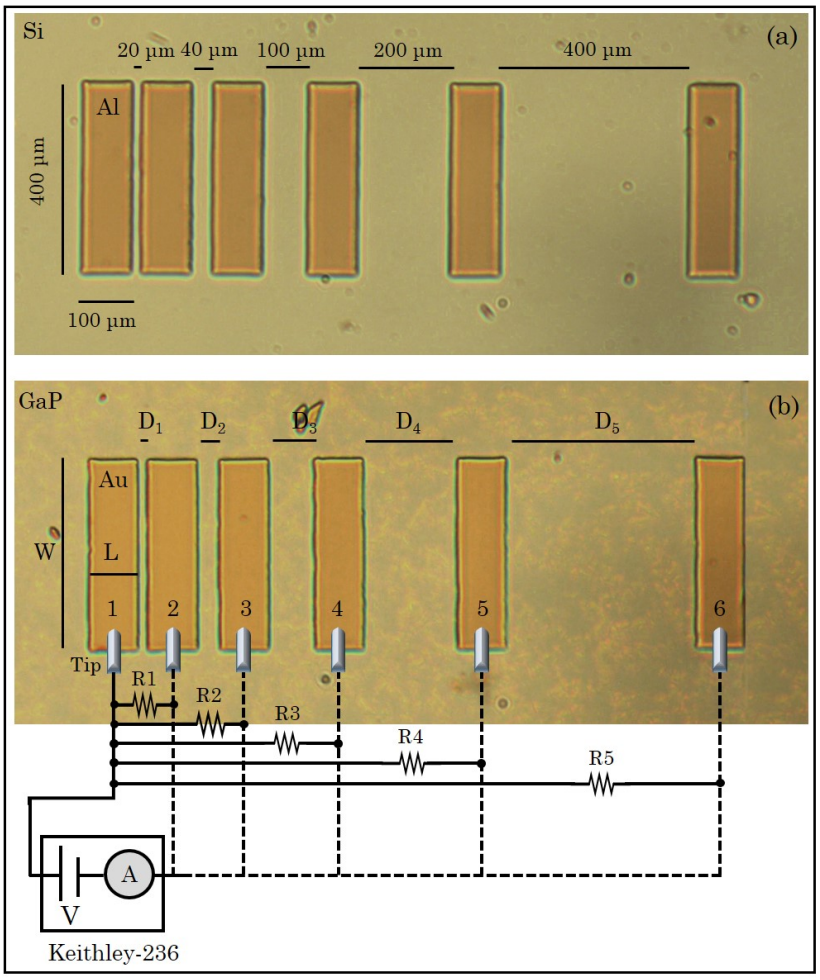

Figure 6.31: *Ohmic-contact image and resistance measurement configuration for (a) Al/Ni contacts on the Si substrate and (b) Au-Ge/Ni contacts on the GaP layer.*

The contact resistance is measured using transmission line measurement (TLM) method [Sta-06]. The first tip is fixed on the pad-1, for example, and the other is changed from 2nd to 6th pad. Accordingly, the resistance between two pads will change from R_1 to R_5. The resistance (R_T) between the two pads is given by

$$R_T = 2R_c + R_s, \tag{6.2}$$

where R_c is the contact resistance and R_s is the semiconductor resistance. With the increase of separation between the pads, R_T increases as well. That means, $R_T = R_1$ or $R_T = R_2$ for the measurement between pad-1 and pad-2, or pad-1 and pad-3, respectively. According to TLM method, a number of resistance measurements versus separation between each pair of contacts must be achieved to plot TLM graph. The plot is linear whose slope gives the resistance of semiconductor, and the

intercept with the y-axis gives $2R_c$. Figure 6.32 demonstrates such graph for the Ohmic resistance of Au/Au-Ge contact on the GaP layer. Therefore, at zero-length resistor, i.e. D = 0, $R_T = 2R_c$, because R_s in Eq. 6.2 becomes zero. From this figure, the resistance of Au-Ge/Ni contact was calculated to be 2.55 Ω. Similarly, the Al-contact resistance was found to be 3.56 Ω.

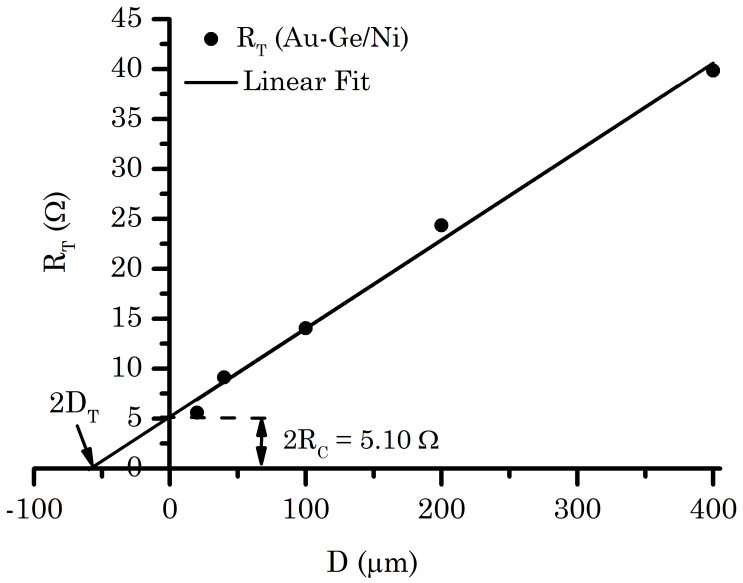

Figure 6.32: *Transmission line measurement for Au-Ge/Ni contact of thickness of 100 nm evaporated on the Gap layer. $2R_c$ is equal to 5.1 Ω, and consequently the contact resistance is 2.55 Ω.*

The contact resistance can be calculated by [Sze-07]

$$R_c = \frac{\rho_c}{W D_T}, \tag{6.3}$$

where ρ_c is the specific contact resistance measured in $\Omega.cm^2$, W is the width of the pad and D_T is the transfer length. D_T is defined as the average distance required for an electron/or hole to travel in the semiconductor beneath the contact before reaching the contact, and defined as [Yu-02]:

$$D_T = \sqrt{\frac{\rho_c}{R_s}}. \tag{6.4}$$

Substituting Eq. 6.4 and Eq. 6.3 in Eq. 6.2 yields

$$R_T = \frac{R_s}{W}(D + 2D_T). \tag{6.5}$$

Equation 6.5 demonstrates that the intercept of the line of Fig. 6.32 with the x-axis gives $2D_T$, which is equal to $-57\ \mu m$. Thereby, ρ_c can be calculated by

$$\rho_c = R_c W D_T. \tag{6.6}$$

ρ_c is found to be 2.56 $\times 10^{-4}\ \Omega.cm^2$ for Au-Ge/Ni contact, and 5.62 $\times 10^{-4}\ \Omega.cm^2$ for Al/Ni contact.

6.10 Electrical Properties of the Nanodiodes

After fabricating the metallic contacts, $I-V$ measurements for the diode array were carried out using the setup described in Sec.4.5.1. These measurements were performed at a temperature range from 300 to 500 K. Figure 6.33 illustrates $I-V$ characteristics for the GaP/Si nanodiode array. The inset figure is related to the room-temperature measurement. The forward $I-V$ characteristics show no significant change at different temperatures. From the room-temperature forward characteristics, the nanodiodes parameters; η, V_b, R_s were extracted using the same method mentioned in Sec. 5.6.2.

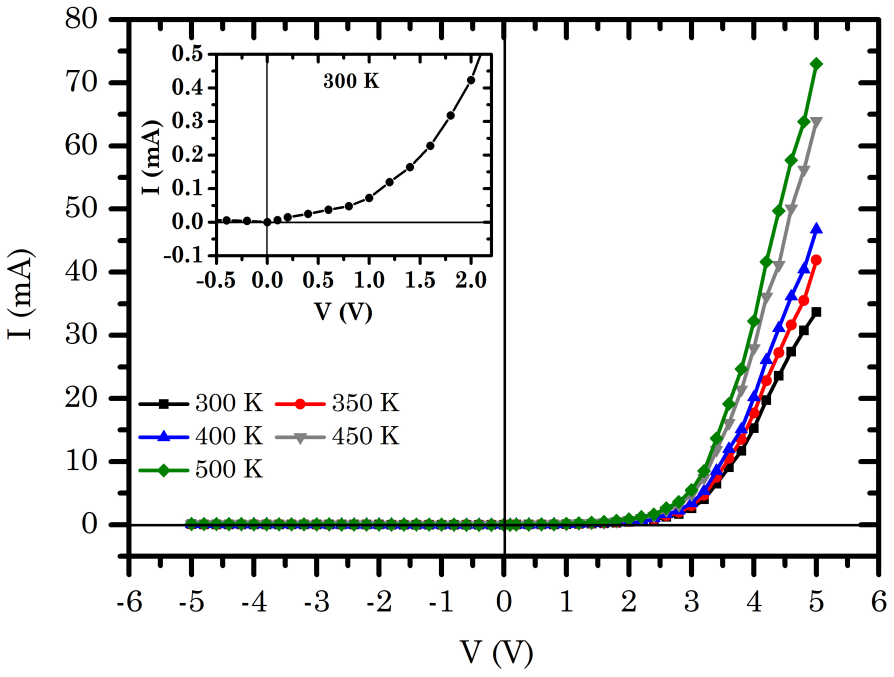

Figure 6.33: *The $I-V$ characteristics of the GaP/Si nanodiode array measured at a temperature range of 300 - 500 K. The inset plot is related to the room-temperature $I-V$ characteristics.*

The values of η, V_b and R_s were calculated to be 1.5, 0.59 V and 482 Ω, respectively.

The electric conductivity of the nanodiode array was calculated to be 5.19 $(\Omega cm)^{-1}$, using the formula $\sigma = d/AR_s$ (Sec. 5.6.2), with $d = 0.040045$ cm and $A = 1.6 \times 10^{-5}$ cm^2. The array conductivity is thus decreased comparing to the heterostructure sample S6:1903 with the same area. This may be caused by the increase of the series resistance.

Besides that, as shown in Fig. 6.34 the reverse current passing through the diode array show a little increment due to temperature increment. This can be explained in terms of producing more minority carriers that across the junction. The room-temperature reverse current was estimated to be 139 nA.

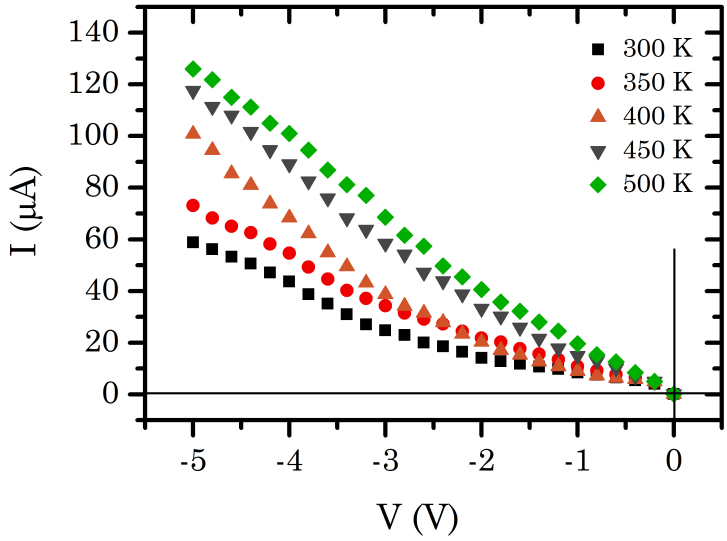

Figure 6.34: *The reverse $I-V$ characteristics of GaP/Si nanodiode array measured at a temperature range of 300 - 500 K. The higher temperature the higher reverse current is observed.*

The carrier transport mechanism of the nanodiodes can be better understood via log-log $I-V$ characteristics plot. Such plot for the room-temperature GaP/Si nanodiode array is demonstrated in Fig. 6.35. The experimental data is compared with the simulated curve of $I = aV$, where a is a normalized constant. In this plot two different conduction regions can be identified: $I \backsim V$ and $I \backsim exp(V)$, In the low region, the forward current passing through HJ nanodiodes is linearly dependent on the bias voltage, exhibiting an ohmic behaviour. Here, due to low-bias voltage the carriers injected from n-region to p-region are somewhat few, and hence the plot approximately matches the simulated plot ($I = aV$). When the bias voltage is increased, the injected carriers are considerably increased, and hence the forward current increases approximately with the exponential value of the bias

voltage, presenting a thermionic emission diode characteristic[Li-06]. Hence, the $I-V$ plot follows $I \backsim exp(V)$.

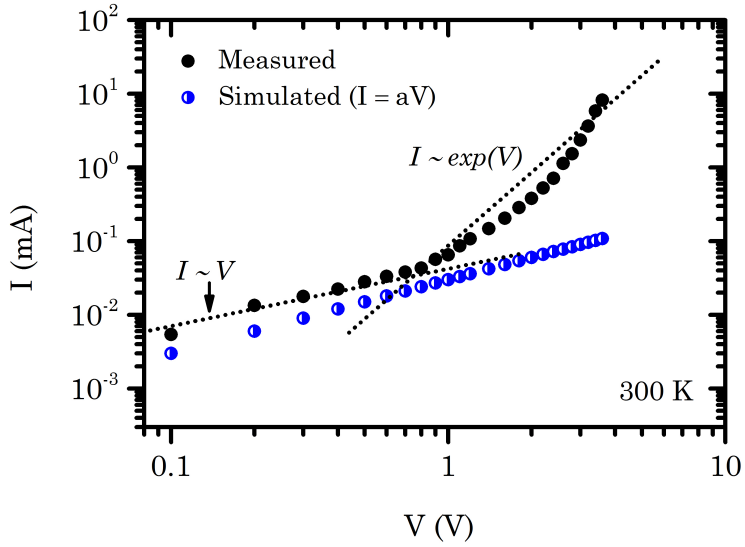

Figure 6.35: *Room-temperature Log-log $I-V$ characteristics of the GaP/Si nanodiodes. Simulated curve of $I = aV$ is compared with the experimentally collected data (a is constant). The practical curve matches $I \backsim V$ and $I \backsim exp(V)$.*

On the other hand, the existence of impurities, like traps, in the bandgap would necessary change the carrier transport profile. If such a case occurs, the electrons could be captured or released by the traps. As a result, an attenuation in the forward current will take place, and thence the log-log $I-V$ curve shows a quadratic dependence, indicating a space-charge limited current mechanism. Since there is no region of quadratic dependence of current on the voltage ($I = V^2$), $I-V$ characteristics of the nanodiodes confirm the absence of traps in the bandgap.

Also, the electrical properties confirm an improvement in the quality factor relative to the bulk GaP/Si diode. The quality factor acts as a measure for the crystal quality of the device. That means, the crystal quality is thus improved in the nanodiodes. This finding might be explained in terms of diminishing some of the defects due to etching of regions containing the defects.

6.11 LFN Measurements of the Nanodiodes

Low-frequency noise measurements for the GaP/Si nanodiode array were also carried out in the frequency range from 10 Hz to 100 kHz at different temperatures, using the same setup described in Sec 5.8. The collected time-domain measurements were converted to frequency-domain using Welch's method. The room-temperature

PSD spectra for the GaP/Si nanodiodes biased with a forward current changes from 10 to 100 μA are illustrated in Fig. 6.36. This figure shows typical LFN spectra including $1/f$ noise components and terminated with white noise components. Also, with increasing the bias current, the flicker noise component increases accordingly, where $S_I \backsim I^2$. Therefore, the highest spectrum level is correlated to the highest current. Moreover, all the spectra are well fitting to $1/f$ noise, and free of $G-R$ noise components.

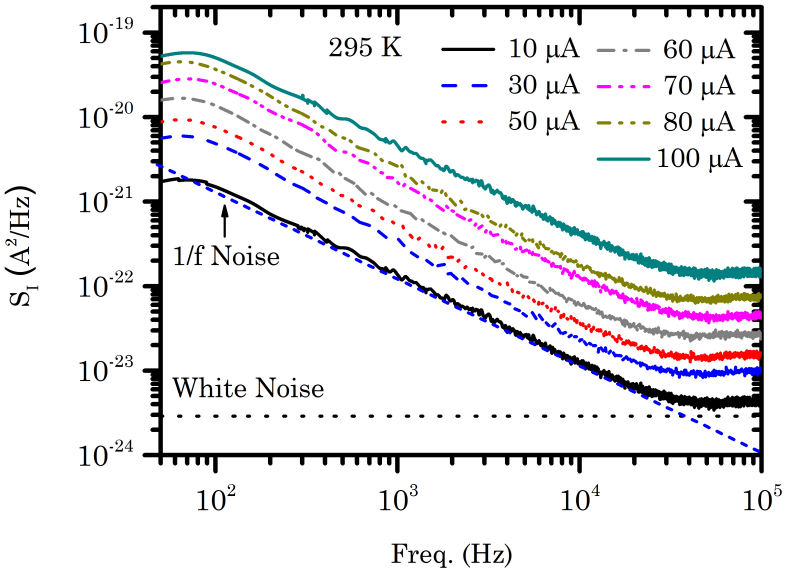

Figure 6.36: *Room-temperature PSD spectra of the GaP/Si nanodiode array measured at a bias current ranging from 10 to 100 μA. All the spectra are fitting to the pure $1/f$ noise, with different white noise levels.*

6.11.1 Temperature-Dependent LFN Measurements

To boost the free-trap bandgap nanostructures, high and low-temperature LFN measurements were achieved. Figure 6.37 shows a comparison between the PSD spectra for the GaP/Si sample S6:1903 and the nanodiodes biased with a forward current of 100 μA and measured at temperatures of 360 K and 80 K. Since there is no existence of Lorentizian components in the spectra, these measurements are considered another evidence for the absence of traps in the bandgap of the nanodiodes.

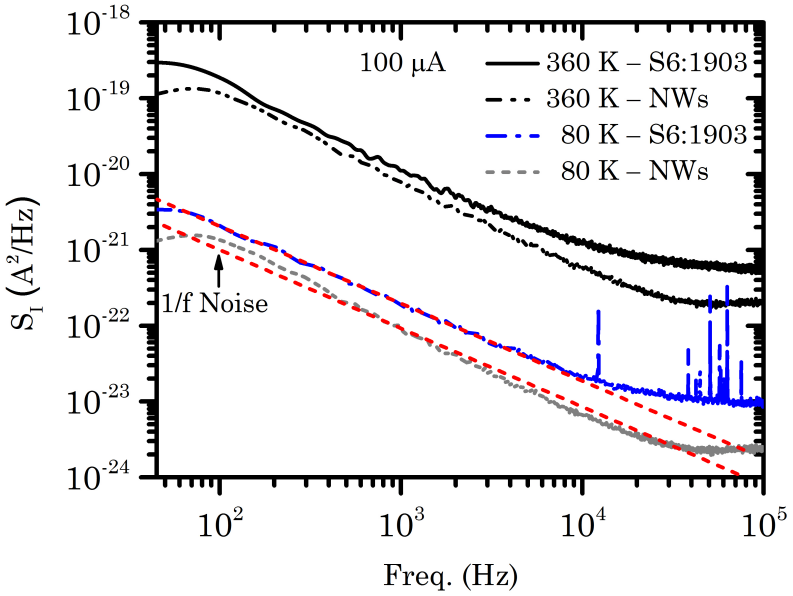

Figure 6.37: *Comparison between the PSD spectra of the GaP/Si sample S6:1903 and the nanodiodes biased with a current of 100 μA and measured at 360 K and 80 K. Both the nanodiodes spectra have lower level than that measured in the bulk diode.*

6.11.2 White-Noise Components

As seen in Fig.6.37, the white noise levels corresponding to both temperatures are much decreased in the nanodiodes comparing to the bulk. One acceptable interpretation goes back to the higher resistance of the diode array, which lowers the thermal noise. In fact, the white noise presented at the tail of the spectrum is composed of thermal and shot noise. If we consider the noise background of the electronic components of the used setup approaches zero volt, the thermal noise can be calculated from the measured resistance at a given current using Johnson-Nyquist noise formula (Eq. 2.15). The white noise for the sample S6:1903 and the nanodiodes are illustrated in Fig. 6.38. Obviously, the white noise is much higher than thermal noise and decreases at higher resistance. Therefore, it is reasonably to expect that the lower level of the nanodiodes white noise is attributed to the decrease in the thermal noise and the shot noise too. The decrease in the shot noise is believed due to suppressing of some defects during etching. At low current, the shot noise is decreased, and therefore the white noise becomes very close to the thermal noise. This case is inverted at higher current, where both the shot noise and thermal noise increase.

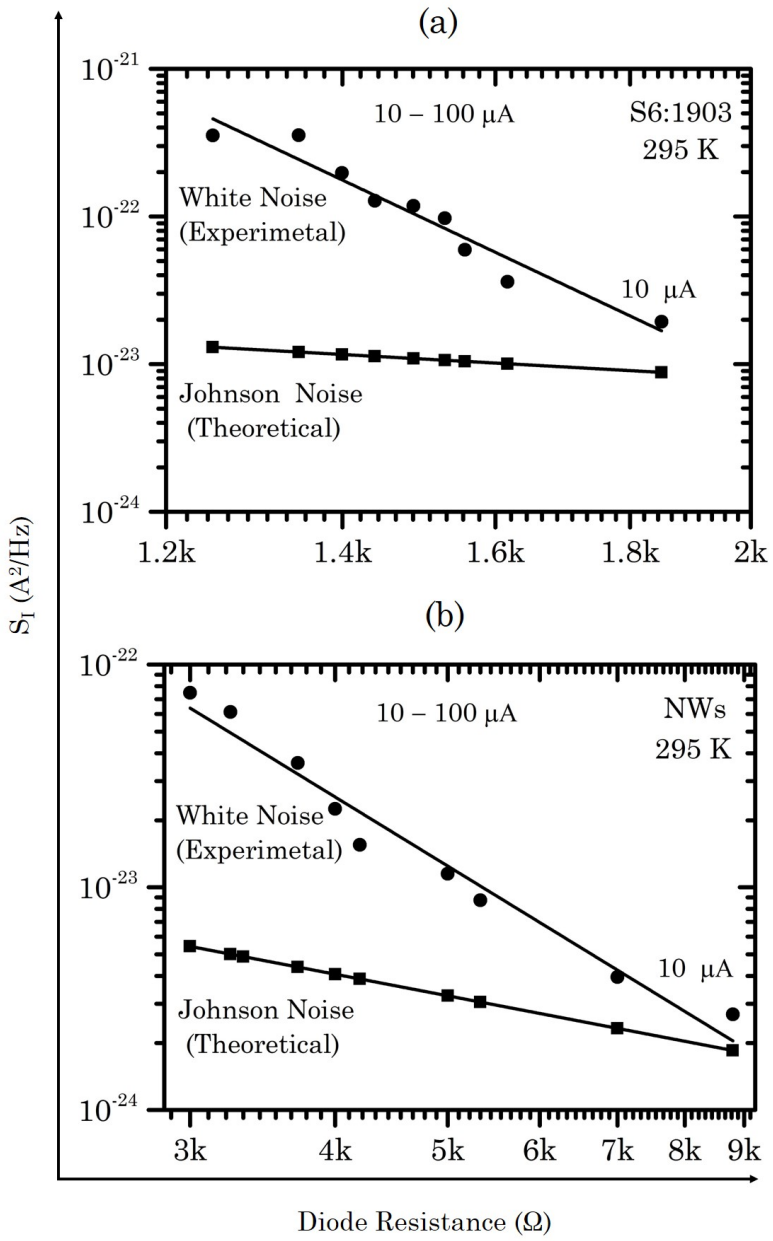

Figure 6.38: *The white noise components of the GaP/Si sample S6:1903 and nanodiode array corresponding to a bias current range from 10 to 100 μA and measured at room temperature. The white noise level of the nanodiodes is lower than that measured in the bulk diode.*

6.12 Conclusion

The nanoscale e-beam resist patterns, reported in this chapter, are dependent on many parameters: e-beam energy, e-beam dose, beam spot-size and the substrate

surface. At higher accelerating voltage, 17 kV, the PMMA pattern was found to be distorted. Because of high-energy electrons, the PMMA chains are more broken producing more fragments at the walls of the exposed area. Therefore, during developing the resist, some of the fragments polymerize causing a distortion in the pattern [Moh-11].

When the beam spot-size is chosen to be 50 nm, the printed feature is broadened due to increase of the divergence of the beam. Additionally, if the dose is higher or lower than the optimal dose, the feature either becomes bigger than the designed pattern or the lift-off process will fail. This occurs as a result of proximity effect that increases with higher dose, and thereby the PMMA pattern is distorted in addition to create a V-type process in the hole walls. Due to astigmatism, the holes of the pattern have an oval shape. Correction of the astigmatism produces high contrast pattern.

Finally, gold nanopattern of hole density about 1.5 $\times 10^8 cm^{-2}$ with diameters of the order of 200 nm on the GaP substrate and the GaP/Si films were obtained. The systematic parameters were optimized at V_{ac} of 12 kV, EB dose of 130 $\mu C/cm^2$, S_P of 25 nm and Mag of 1800$\times$ on a PMMA resist of thickness of 190 nm.

Nanodiode array based on GaP nanowires of diameters about 200 nm were fabricated and characterized. The electrical properties of the device confirm the $I-V$ rectification characteristics with lower quality factor. Thereafter, LFN measurements were carried out, which confirm the absence of the $G-R$ processes, and decreasing the level of $1/f$ and white noise in comparison to the bulk diode.

CHAPTER-7

Conclusion

Conclusion

7.1 Conclusion

The research reported in this thesis includes some practical steps starting from the growth of GaP/Si heterostructures, followed by the fabrication of gold nanopatterns on the grown films using e-beam lithography. Benefiting from the MacEtch method, GaP/Si nanowires were successfully fabricated. The nanowires were used for the fabrication of low-noise nanodiode array.

GaP films were grown on Si substrates using a Riber-32P gas-source molecular-beam epitaxy system. Their growth conditions, including growth temperature, epilayer thickness and thermal annealing were optimized. The optimal growth temperature and the layer thickness were determined to be 400 °C and about 500 nm, respectively. After terminating the growth process, some of the films were subjected to a thermal annealing initiating from the growth temperature under PH_3 flux. Two methods were employed and then compared. In the first well-known method, the temperature is increased from the growth to annealing temperature instantaneously, and lasts for a certain time. The second method has recently been proposed in this thesis, at which the temperature is raised step-by-step at a rate of 8 °C per 5 min, and we referred to as SGA. Because of the large difference in the thermal expansion coefficients between GaP and Si, the layer is energetically favoured to relax. Hence, in the proposed method, the strain of the layer increases slowly and resists the relaxation during annealing and on cooling to room temperature. This finally led to retain more residual strain in the layer. A comparison between both methods confirmed that the samples annealed by SGA showed a high improvement in the structural properties of the layers. Accordingly, the density of dislocations generated due to layer relaxation was decreased in the GaP/Si samples due to SGA.

The epilayers of most of the samples were found to be n-type auto-doped. Such feature was already observed in MOVPE GaP/Si [Dix-06] and interpreted to the diffusion of Si atoms in the GaP layer. In our system, the auto-doping was attributed to either diffusion of Si atoms in the GaP layer, or the layer was doped by diffusion of phosphorus atoms during annealing, or both mechanisms might possibly arise. This allowed for the fabrication of $p-n$ heterojunction diodes.

It is well-established that transport properties are strongly related to the existence of the dislocations, since they could interact to form trap levels. Characterization of the films grown at 400 °C pointed to the existence of deep levels in the unannealed films. However, the comparison between the unannealed and annealed films confirmed that the transport properties of the heterostructures were improved due to SGA.

Using LFN spectroscopy to characterize the GaP/Si films enables to figure out the role of thermal annealing to suppressing many defects. The spectra were analyzed and the Hooge parameters of the films were extracted, which were of the order

of 10^{-3} to 10^{-5}. Again, we observed that the level of the current noise spectral density was decreased under the influence of SGA, and the Hooge parameter has a lower value. Furthermore, the trap levels formed in the energy gaps were found to be diminished. The most possible reason behind that is the deep levels could permanently be filled by electrons during annealing.

On the GaP/Si surface, e-beam lithographic nanopatterns were printed. Although at beginning the printing process of the nanopatterns was optimized to GaP substrates because the surface was very smooth, gold-mesh nanopatterns were successfully then transferred to the surface of the heterostructure films.

Eventually, the systematic parameters of lithography that include an accelerating voltage of 12 kV, an e-beam dose of 130 $\mu C/cm^2$ and a PMMA resist thickness of 190 nm were optimized. Consequently, a high-density gold nanopattern of holes, with diameters of the order of 200 nm, were successfully fabricated on the GaP substrate and the GaP/Si films.

Thereafter, MacEtch of GaP was experienced using a solution of HF/$KMnO_4$ with different concentrations at different temperatures. It was found that the ratio of the vertical to the lateral etching was increased at a concentration ratio around (2 M)HF/(10 mM)$KMnO_4$, and at a temperature about 45 °C. Alternatively, when the concentration of $KMnO_4$ was much increased, inverted MacEtch occurred. In this case, the solution might attack GaP, while the region under gold can be protected by the gold itself producing vertical nanostructures by using a gold-dot pattern. A nanowire array of diameter about 200 nm and density between 1 and 3×10^8 cm^{-2} was obtained from the MacEtch of GaP.

Ohmic contacts of Au-Ge/Ni and Al/Ni were evaporated on the GaP layer and the Si backside, respectively. Their specific resistances were then estimated to be 2.56×10^{-4} $\Omega.cm^2$ and 5.62×10^{-4} $\Omega.cm^2$. Thereby, nanodiode array was fabricated and characterized using the electrical and LFN measurements. According to the electrical properties for the nanodiodes, $I-V$ rectification characteristic was confirmed, as well as the quality factor was reduced relative to the annealed sample. The LFN measurements indicated that the $G-R$ noise processes generated by the traps in the energy bandgap were not observed, and the $1/f$ noise levels were reduced relative to the bulk diode.

It is concluded that the GaP nanodiodes fabricated by this method can be used for low-noise applications.

7.2 Future Researches

To the best of our knowledge, the GaP/Si nanodiode array is the first attempt fabricated by MacEtch. Of course, this device can't satisfy all the requirements for low-noise nanodevices, and needs more developments. However, some of future

works may be possible based on this research such as:

1. Study the ability to minimize the hole size to sub tens of nanometers to study the effect of energy band confinement on the electrical and optical properties of the fabricated nanowires.

2. Increase the working area by fabricating photographic mask from the e-beam lithographic pattern so as to increase the density of nanostructures, which may enable studies for detector applications.

3. It may be possible to fabricate different types of nanostructures, such as nanocapacitors from GaP substrates or GaP epilayers using the similar process presented in this thesis.

4. A GaP field-effect transistor array for high-temperature applications may possibly be fabricated from GaP substrate using the same method by adding a metallic gate between the contacts of the nanowires.

Appendices

Appendices

A.1 Power Spectral Density

The power spectrum detects the existence of repetitive patterns in a random noise signal. In other words, power spectral density (PSD) characterizes the distribution of the power of a signal in frequency domain. PSD is important to give an understandable interpretation of a random signals for a wide range of applications, such as signal detectors, radar and etc. Various methods have been introduced for estimation of PSD: Bartlett, Blackman & Tukey and Welch methods [Kal-13]. The later has been widely employed for computing PSD since 1967 [Wel-67]. While The fast Fourier transform (FFT) was submitted by Cooley and Tukey [Coo-65], Welch's method becomes widespread, because it provides an efficient computation for the estimation of PSD [Gup-13, Rah-14]. Various programs and scientific software have been proposed for this purpose other than MATLAB, such as C++ Language, signal processing algorithms, and etc. Here, with aid of Matlab-Verion R2013a, a PSD is estimated using Welch's method.

A.1.1 Discrete Fourier Transform

Consider a finite-time signal $x(m)$ of length N samples, the discrete Fourier transform (DFT) can be defined as N equally spaced spectral samples as [Dju-99, Vas-20]:

$$X(n) = \sum_{m=0}^{N-1} x(m) e^{(-j2\pi/N)mn}, \qquad n = 0, ..., N-1 \tag{A.1}$$

This is satisfied for all signals. For instance, speech signals are composed of short-duration sounds varied with the time. With the use of the DFT, spectral characteristics of each short interval are possibly recognized by the user. Therefore, it is recommended to take a somewhat enough time of measurements to allow higher resolution signals.

Consider a window of N equally spaced time-domain samples represented by [x(0), x(1), ..., x(N-1)], with duration $\Delta T = N.T_s$, is used as an input for the DFT, then the output is also N spectral samples in frequency-domain separated between 0 Hz and sampling frequency $F_S = 1/T_S$ Hz. The frequency separation between two successive points (Δf) is given by

$$\Delta f = \frac{1}{\Delta T} = \frac{F_S}{N} \tag{A.2}$$

A.1.2 Fast Fourier Transform

Various methods have been proposed to calculate the discrete Fourier transform. One of the most used for this purpose is referred to as the fast Fourier transform.

The idea of the FFT is based on the fact that an N point time-domain signal is decomposed into N signals in time-domain depending on the binary number system 2^N. For example, a 32-point signal can be divided into two signals each of 16 points. The second signal is also divided into two signals with 8 points, and so forth. Finally, the frequency-domain spectra are calculated from these points.

A.1.3 Estimation of the Power Spectral Density

PSD represents the distribution of the signal power in the frequency-domain, and defined as:

$$\left|X(f)\right|^2 = \left|\sum_{m=-\infty}^{\infty} x(m)e^{-j2\pi fm}\right|^2, \tag{A.3}$$

and by using the classical periodogram method, the PSD of an N sample can be estimated by [Vas-20]

$$Px(f) = \frac{1}{N}\left|\sum_{m=0}^{N-1} x(m)e^{-j2\pi fm}\right|^2, \tag{A.4}$$

where $Px(f)$ is an expression for PSD. The later is abbreviated to the form below:

$$Px(f) = \frac{1}{N}\left|X(f)\right|^2. \tag{A.5}$$

In this equation, the PSD function is the basis estimation of non-parametric methods.

A.1.3.1 Welch's Method for the Estimation of PSD

One of the averaging periodograms is the Welch Method. In this method, the signal $x(m)$, whose length is N samples, can be divided into K overlapping segments each of length M. For i^{th} segment, the signal can be given as

$$x_i(m) = x_i(m + iV), \qquad m = 0, ..., N-1,\ i = 0, ..., K-1, \tag{A.6}$$

where V is the overlap number. If there is no overlap, $V = N$, while $V = N/2$ for half overlap. Also, each segment must be windowed in $w(m)$ before estimating the periodogram. In this case, $Px(f)$ for each segment is expressed by [Vas-20, Kal-13]

$$P^i x(f) = \frac{1}{NW}\left|\sum_{m=0}^{N-1} w(m)x(m)e^{-j2\pi fm}\right|^2, \tag{A.7}$$

where W is the length of the window, calculated by

$$W = \frac{1}{N}\sum_{m=0}^{N-1} w^2(m), \tag{A.8}$$

A.1.3.2 Matlab Code of the Power Spectral Density

PSD for noise signals recorded from the GaP/Si films is estimated by Matlab program using FFT syntax. Below is the program code of PSD.

A MATLAB CODE FOR ESTIMATION OF POWER SPECTRUM DENSITY USING WELCH METHOD. (SOFTWARE USED : MATLAB R2013a)

```
clc
close all
load file.csv;                          Load Data File to MATLAB
x = load ('file.csv');
T = x(:,1);                             T: Time of Input Signal
I = x(:,2);                             I: Current of Input Signal
xlabel('t (sec)');
ylabel('I1 (A)');
Ts = 1e-5;                              Sampling Time
Fs = 1/Ts;                              Sampling Frequency
L = length(x)                           Length of Signal
nfft = 2^nextpow2(L)                    Approaches Signal Length
                                        to the Next Higher 2^L
D = ('Type Length of Segment:');        Enter Length of Each Segment
M = input(D);
W = hanning(M);                         Use Hanning Window
K = fix(L/M)                            Compute the Digital Number of Segments
A = K.*M
K1 = fix((2.*L/M)-1)                    Compute Number of Overlapping Segments
S = sum(W.^2);                          Length of Window
P = zeros(nfft,1);                      Create A Matrix and Store Elements
for j = 1:K1;                           Estimation of PSD Using FFT Syntax
q = (M/2)*(j-1) + 1;                    Overlap = 50%
Px = fft(I(q:q+M-1).*W, nfft);
Pxx = (abs(Px).^2)/(Fs*S);
P = P + Pxx;
end
Psd = P/K1;
Psd1 = Psd(1:A);                        PSD for Length of K1xM Only
df = Fs./A                              Frequency Separation Between
Two consecutive points
f = [1:A]*df;
figure(1);
loglog(f,Psd1);grid
```

```
axis([1 2e5 1e-24 1e-19]);
xlabel('Freq. (Hz)')
ylabel('S_I (A^2/Hz)')
title ('Welch's Method of Power Spectral Density Estimation');
X =reshape(f,[A,1]);                    Save PSD As ASCII File
Y =reshape(Psd1,[A,1]);
dlmwrite('fileSpd.txt',[X,Y],'delimiter', '');
```

A.1.4 Extraction of Low-Frequency Noise Components

Consider the LFN spectrum is shown in Fig. A.1. For simplicity, we consider there is just one $G-R$ noise process, and thence the spectral noise density is given by

$$S_I(f) = \frac{A_{1/f}\ I^2}{f} + \frac{B\ I^2}{1+(f/f_{G-R})^2} + White\ Noise, \tag{A.9}$$

where $A_{1/f}$, B and f_{G-R} are the flicker noise amplitude, the $G-R$ noise amplitude and the characteristic frequency of the $G-R$ noise, respectively.

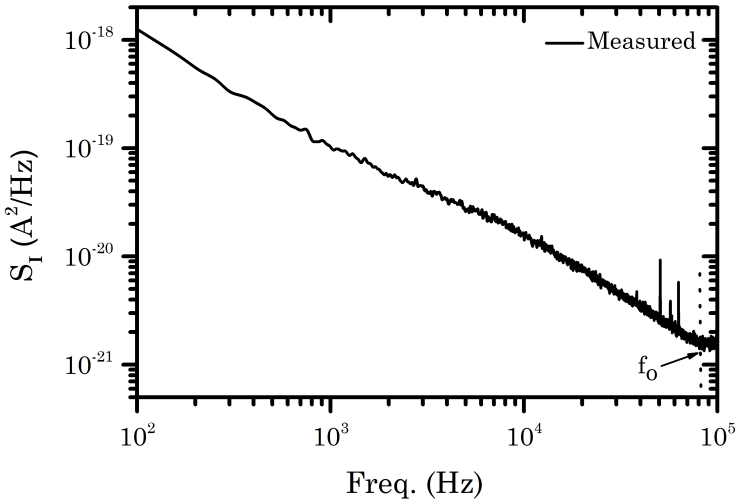

Figure A.1: *Power spectral density spectrum for a GaP/Si sample*

In order to extract the spectrum components, we first deal with the $1/f$ component in Eq. A.9:

$$S_I(f) = \frac{A_{1/f}\ I^2}{f} \tag{A.10}$$

This equation can be written in a simple form as

$$S_I(f) = \frac{D}{f} \tag{A.11}$$

where $D = A_{1/f}I^2$. The value of D is simply obtained by fitting Eq. A.11 to the PSD spectrum. If there is no $G-R$ noise component, then Eq. A.9 has just two terms; $1/f$ and white noise components. In this case, $1/f$ must be absolutely fitting the PSD spectrum down to characteristic frequency $f_\circ$. Otherwise, the curve will show a deviation from this component due to $G-R$ noise component. However, the extracted value of $A_{1/f}$ is then substituted in Eq. A.10 to get the $1/f$ component,

as shown in Fig. A.2. One can see that the $1/f$ component is not fitted to the spectrum, which confirms the existence of $G-R$ noise.

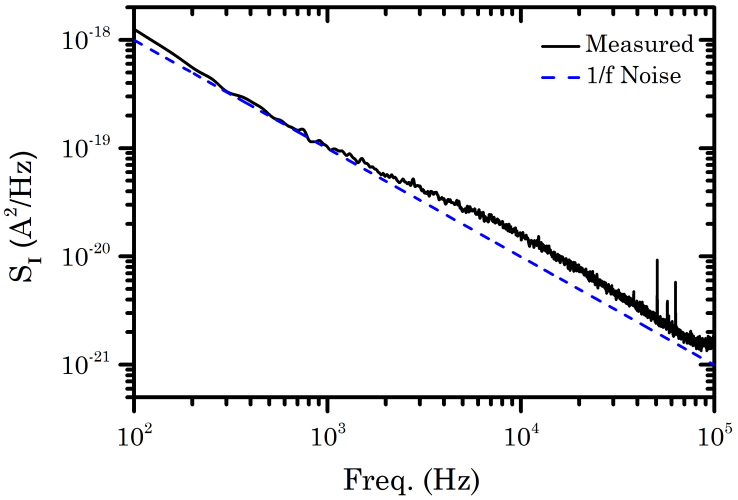

Figure A.2: *PSD spectrum for a GaP/Si sample with a $1/f$ component.*

By subtracting the $1/f$ component from the whole spectrum, the white noise and $G-R$ noise components will be determined, as shown in Fig. A.3.

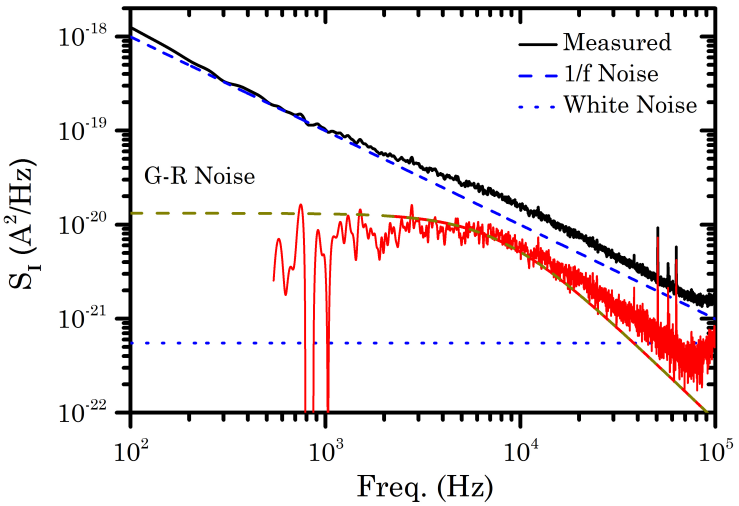

Figure A.3: *PSD spectrum for a GaP/Si sample with $1/f$, $G-R$ and white noise components.*

Then, the f_{G-R} of the $G-R$ noise component can be determined from the normalized PSD spectrum shown in Fig. A.4, which is equal to 7.94 kHz. By fitting the second term of Eq. A.9, or doing Lorentzian fitting for the $G-R$ curve of Fig. A.3 at frequency f_{G-R}, the value of B can be determined, and consequently the fitted

curve of the $G-R$ noise component can be obtained.

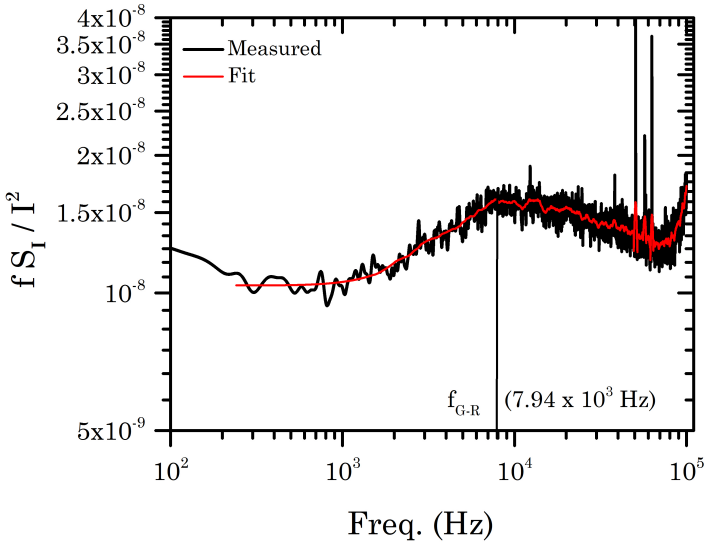

Figure A.4: *The normalized PSD spectrum for a GaP/Si sample, by which the characteristic frequency is determined to be 7.94 kHz.*

In order to make sure that all the components are perfectly extracted, addition of these components should produce the whole spectrum. Figure A.5 shows all the components with the curve produced from the addition, in which the fitting looks very well.

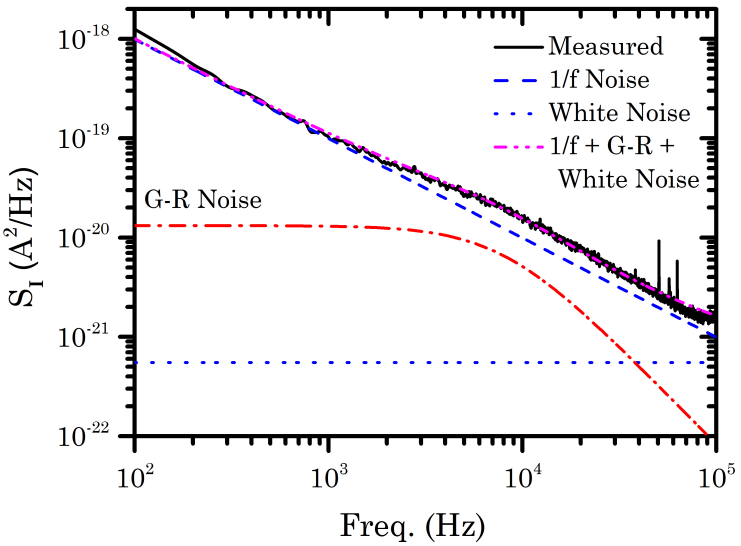

Figure A.5: *The extracted PSD spectrum for a GaP/Si sample. Three components are obtained: $1/f$, $G-R$ and white noise components.*

A.2 Calculation of Molarity

Molar concentration, also referred to as Molarity (M), is defined as the number of moles of a solute per unit volume (V) of a solution. It is mathematically expressed as

$$M = \frac{W}{mV}, \tag{A.12}$$

where W and m are the weight and molar mass of solute measured in (gm) and (gm/mole), respectively. If V is measured in liter, then the unit of M is given by Molar (where Molar = mol/Lit). For example, to get 10 mM of $KMnO_4$, whose m is equal to 158.034 gm/mole, one must dilute 197.54 gm in 125 mL of H_2O. Off course, this weight might be increased or decreased, and thereby the volume of the water must also be changed to get the same molarity.

A.2.1 Calculation of An Acidic Solution Molarity

If the stock solution is acid, such as HF, its molarity can also be calculated from Eq.(1). W represents the mass of acid calculated as below:

$$W(gm) = V \times Strength\ of\ solution\ \%\ (mL) \times Density\ (gm/mL) \tag{A.13}$$

In this equation the volume of the acid is multiplied by its strength percent. For example, when 1mL of 98 % H_2SO_4 is diluted in 10 mL H_2O, then

$$W = 1mL \times 98\% \times 1.84 \text{ gm/mL} = 1.803 \text{ gm.}$$

Substituting this value into Eq.(A.12), we get

$$M = \frac{1.803\ gm}{98.08\ gm/mol \times 0.01\ L} = 1.83\ mol/Lit \tag{A.14}$$

A.3

List of Abbreviations

V_{ac}	Accelerating voltage of the electron beam
Al	Aluminium
AFM	Atomic-force microscope
V_b	Built-in voltage of diode
$C-V$	Capacitance-voltage
CTE	Coefficient of thermal expansion
$I-V$	Current-voltage
DI	Deionized water
DUT	Device under test
K_I	Diffracted wave vector
$e-beam$	Electron-beam
EBL	Electron-beam lithography
EBR	Electron-beam resist
E_D	Energy of dislocations
E_g	Energy gap
E_R	Etching rate
Fac	Factor
E_F	Fermi energy
Ga	Gallium
GaP	Gallium phosphide
$GSMBE$	Gas-source molecular-beam epitaxy
$G-R$	Generation-recombination
Au	Gold
$GEXRD$	Grazing exit X-ray diffraction

$GIXRD$	Grazing incidence X-ray diffraction
HJ	Heterojunction
W	Heterojunction width
HS	Heterostructure
HLE	High-level electronic unit
HCl	Hydrochloric acid
HF	Hydrofluoric acid
H_2O_2	Hydrogen peroxide
$K_\circ$	Incident wave vector
In	Indium
Q_x	In-plane Cartesian coordinate of reciprocal-space map
E_H	Letral-etching rate
LFN	Low-frequency noise
LLE	Low-level electronic unit
Mag	Magnification of scanning-electron microscope
$MacEtch$	Metal-assisted chemical etching
$MIBK:IPA$	Methyl isobutyl ketone:isopropanol alcohol
NWs	Nanowires
N_2	Nitrogen gas
Q_z	Out-of-plane Cartesian coordinate of reciprocal-space map
P	Phosphorus
PH_3	Phosphine gas
$PMMA$	Polymethyl methacrylate electronic-beam resist
$KMnO_4$	Potassium permanganate
RSM	Reciprocal-space mapping
$RHEED$	Refection high-energy electron diffraction
RMS	Root-mean square
R_T	Resistance between two metal contacts
R_C	Resistance of metal contact

R_S	Resistance of semiconductor
SEM	Scanning-electron microscope
K	Scattered wave vector
SMU	Source-measure unit
S_p	Spot size of the electron-beam
SGA	Step-graded annealing
H_2SO_4	Sulfuric acid
t_r	Thickness of electron-beam resist
US	Ultrasonic cleaner
VLS	Vapour-Liquid-Solid
E_V	Vertical-etching rate
W_d	Working distance of lithographic area
XRD	X-ray diffraction

List of Symbols

$A_{1/f}$	Amplitude of flicker noise spectrum
B_i	Amplitude of $G - R$ noise
μ	Attenuation coefficient
$a_\perp$	Out-of-plane lattice parameter
a_L	Unstrained lattice parameter of layer
$a_\parallel$	In-plane lattice parameter
α_H	Hooge factor
α_L	Tilt angle of layer respect to substrate
α_{Si}	Thermal expansion coefficient of Si
α_{GaP}	Thermal expansion coefficient of GaP
c_{11}	Elastic constant of GaP
c_{12}	Elastic constant of GaP
ΔE_C	Discontinuity of conduction band
ΔE_V	Discontinuity of valence band
Δf	Frequency bandwidth
ΔT	Difference in temperatures
$\Delta\alpha$	Difference in thermal expansion coefficients
$\Delta\theta$	XRD peaks splitting between the substrate and the layer
$\Delta\mu$	Mobility fluctuations
Δn	Free-carrier number fluctuations
δ_L	Inclination angle of the diffraction plane of layer
δ_S	Inclination angle of the diffraction plane of substrate
$\epsilon_\circ$	Vacuum permittivity

ϵ_1	Permittivity of substrate
ϵ_2	Permittivity of layer
ε	Residual strain
ε_M	Strain due to lattice-mismatch
ε_T	Strain due to thermal-mismatch
ε_{Th}	Thermal strain
E_S	Elastic strain energy
E_T	Total strain energy
E_{VAC}	Vacuum energy level
$f_\circ$	Corner frequency of $G-R$ noise spectrum
$1/f$	Flicker noise
h_c	Thickness of layer
$I_\circ$	Reverse saturation current
K	Dielectric constant
k_s	Cantilever spring constant
k	Boltizmann constant
$m_\perp$	Perpendicular lattice mismatch
$m_\parallel$	parallel lattice mismatch
n	Concentrations of free electrons
N	Dislocations density
N_a	Acceptor carrier concentration
N_C	Effective conduction band density state
N_d	Donor carrier concentration
η	Ideality factor of diode
N_V	Effective valence band density state
p	Concentrations of holes
q	Elementary charge of electron
R	Relaxation degree
R_s	Series resistance

r_d	Diode dynamic resistance
S_G	Spectral density of conductance fluctuation
S_I	Spectral density of thermal noise current
S_V	Spectral density of thermal noise voltage
σ	Electric conductivity
σ_T	Thermal stress
θ_S	Bragg's angle of substrate
θ_l	Bragg's angle of layer
T_a	Annealing temperature
T_g	Growth temperature
T_r	Room temperature
μ_I	Mobility due to impurities scattering
μ_L	Mobility due to phonon scattering
μ_n	Electron mobility
μ_p	Hole mobility
μ_S	Mobility due to surface roughness scattering
ν	Poisson ratio
V_T	Thermal voltage
X	Electron affinity

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Selbständigkeitserklärung

Hiermit erkläre ich, die vorliegende Arbeit selbstndig ohne fremde Hilfe verfasst zu haben und nur die angegebene Literatur und Hilfsmittel verwendet zu haben.

Ich habe mich anderwärts nicht um einen Doktorgrad beworben und besitze einen entsprechenden Doktorgrad nicht.

Ich erkläre die Kenntnisnahme der dem Verfahren zugrunde liegenden Promotionsordnung der Mathematisch-Naturwissenschaftlichen Fakultät I der Humboldt-Universität zu Berlin.

Berlin, den 25.10.2016
Emad Hameed Hussein Al-Khushein

Dedicated to

Memory of my father

My mother, my wife and daughters